A10 Port Controller

2011.10

Table of Contents

1. Overview

The chip has 8 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 18 input/output port
- Port B(PB): 24 input/output port
- Port C(PC): 25 input/output port
- Port D(PD): 28 input/output port
- Port E(PE) : 12 input/output port
- Port F(PF) : 6 input/output port
- Port G(PG) : 12 input/output port
- Port H(PH) : 28 input/output port
- Port I(PI) : 22 input/output port
- Port S(PS) : 84 input/output port for DRAM controller

For various system configurations, these ports can be easily configured by software. All these ports (except PS) can be configured as GPIO if multiplexed functions not used. 32 external PIO interrupt sources are supported and interrupt mode can be configured by software.

2. Port Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n from 0 to 9)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n from 0 to 9)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n from 0 to 9)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n from 0 to 9)
Pn_DAT	n*0x24+0x10	Port n Data Register (n from 0 to 9)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n from 0 to 9)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n from 0 to 9)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n from 0 to 9)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n from 0 to 9)

PIO_INT_CFG0	0x200	PIO Interrrupt Configure Register 0
PIO_INT_CFG1	0x204	PIO Interrrupt Configure Register 1
PIO_INT_CFG2	0x208	PIO Interrrupt Configure Register 2
PIO_INT_CFG3	0x20C	PIO Interrrupt Configure Register 3
PIO_INT_CTL	0x210	PIO Interrupt Control Register
PIO_INT_STA	0x214	PIO Interrupt Status Register
PIO_INT_DEB	0x218	PIO Interrupt Debounce Register
SDR_PAD_DRV	0x220	SDRAM Pad Multi-Driving Register
SDR_PAD_PUL	0x224	SDRAM Pad Pull Register

3. Port Register Description

3.1. PA Configure Register 0

Offset: 0x00			**Register Name: PA_CFG0** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PA7_SELECT 000: Input 001: Output 010: ETXD0 011: SPI3_MOSI 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	Reserved
26:24	R/W	0	PA6_SELECT 000: Input 001: Output 010: ETXD1 011: SPI3_CLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PA5_SELECT 000: Input 001: Output 010: ETXD2 011: SPI3_CS0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PA4_SELECT 000: Input 001: Output 010: ETXD3 011: SPI1_CS1 100: Reserved 101: Reserved

			110: Reserved	111: Reserved
15	/	/	/	
14:12	R/W	0	PA3_SELECT 000: Input 010: ERXD0 100: UART2_RX 110: Reserved	001: Output 011: SPI1_MISO 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PA2_SELECT 000: Input 010: ERXD1 100: UART2_TX 110: Reserved	001: Output 011: SPI1_MOSI 101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PA1_SELECT 000: Input 010: ERXD2 100: UART2_CTS 110: Reserved	001: Output 011: SPI1_CLK 101: Reserved 111: Reserved
3	/	/	Reserved	
2:0	R/W	0	PA0_SELECT 000: Input 010: ERXD3 100: UART2_RTS 110: Reserved	001: Output 011: SPI1_CS0 101: Reserved 111: Reserved

3.2. PA Configure Register 1

Offset: 0x04			**Register Name: PA_CFG1** **Default Value: 0x0000_0000**	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0	PA15_SELECT 000: Input 010: ECRS 100: UART1_DSR 110: Reserved	001: Output 011: UART7_RX 101: Reserved 111: Reserved
27	/	/	/	
26:24	R/W	0	PA14_SELECT 000: Input 010: ETXCK 100: UART1_DTR 110: Reserved	001: Output 011: UART7_TX 101: Reserved 111: Reserved

23	/	/	/
22:20	R/W	0	PA13_SELECT 000: Input 001: Output 010: ETXEN 011: UART6_RX 100: UART1_CTS 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PA12_SELECT 000: Input 001: Output 010: EMDIO 011: UART6_TX 100: UART1_RTS 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PA11_SELECT 000: Input 001: Output 010: EMDC 011: Reserved 100: UART1_RX 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PA10_SELECT 000: Input 001: Output 010: ERXDV 011: Reserved 100: UART1_TX 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PA9_SELECT 000: Input 001: Output 010: ERXERR 011: SPI3_CS1 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PA8_SELECT 000: Input 001: Output 010: ERXCK 011: SPI3_MISO 100: Reserved 101: Reserved 110: Reserved 111: Reserved

3.3. PA Configure Register 2

Offset: 0x08			**Register Name: PA_CFG2** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/

6:4	R/W	0	PA17_SELECT 000: Input 001: Output 010: ETXERR 011: CAN_RX 100: UART1_RING 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PA16_SELECT 000: Input 001: Output 010: ECOL 011: CAN_TX 100: UART1_DCD 101: Reserved 110: Reserved 111: Reserved

3.4. PA Configure Register 3

Offset: 0x0C			Register Name: PA_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.5. PA Data Register

Offset: 0x10			Register Name: PA_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
17:0	R/W	0	PA_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.6. PA Multi-Driving Register 0

Offset: 0x14			Register Name: PA_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1

			10: Level 2	11: Level 3

3.7. PA Multi-Driving Register 1

Offset: 0x18			Register Name: PA_DRV1 Default Value: 0x0000_0005
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 16~17) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.8. PA Pull Register 0

Offset: 0x1C			Register Name: PA_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.9. PA Pull Register 1

Offset: 0x20			Register Name: PA_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 16~17) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.10. PB Configure Register 0

Offset: 0x24	Register Name: PB_CFG0 Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0	PB7_SELECT 000: Input 001: Output 010: I2S_LRCK 011: AC97_SYNC 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PB6_SELECT 000: Input 001: Output 010: I2S_BCLK 011: AC97_BCLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PB5_SELECT 000: Input 001: Output 010: I2S_MCLK 011: AC97_MCLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PB4_SELECT 000: Input 001: Output 010: IR0_RX 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PB3_SELECT 000: Input 001: Output 010: IR0_TX 011: Reserved 100: NC 101: Reserved 110: STANBYWFI 111: Reserved
11	/	/	/
10:8	R/W	0	PB2_SELECT 000: Input 001: Output 010: PWM0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PB1_SELECT 000: Input 001: Output 010: TWI0_SDA 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

3	/	/	/
2:0	R/W	0	PB0_SELECT 000: Input 001: Output 010: TWI0_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

3.11. PB Configure Register 1

Offset: 0x28			Register Name: PB_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PB15_SELECT 000: Input 001: Output 010: SPI2_CLK 011: JTAG_CK0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PB14_SELECT 000: Input 001: Output 010: SPI2_CS0 011: JTAG_MS0 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PB13_SELECT 000: Input 001: Output 010: SPI2_CS1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PB12_SELECT 000: Input 001: Output 010: I2S_DI 011: AC97_DI 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PB11_SELECT 000: Input 001: Output 010: I2S_DO3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/

			PB10_SELECT	
			000: Input	001: Output
			010: I2S_DO2	011: Reserved
			100: Reserved	101: Reserved
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
			PB9_SELECT	
			000: Input	001: Output
			010: I2S_DO1	011: Reserved
			100: Reserved	101: Reserved
6:4	R/W	0	110: Reserved	111: Reserved
3	/	/	/	
			PB8_SELECT	
			000: Input	001: Output
			010: I2S_DO0	011: AC97_DO
			100: Reserved	101: Reserved
2:0	R/W	0	110: Reserved	111: Reserved

3.12. PB Configure Register 2

Offset: 0x2C			**Register Name: PB_CFG2** **Default Value: 0x0000_0000**	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
			PB23_SELECT	
			000: Input	001: Output
			010: UART0_RX	011: IR1_RX
			100: Reserved	101: Reserved
30:28	R/W	0	110: Reserved	111: Reserved
27	/	/	/	
			PB22_SELECT	
			000: Input	001: Output
			010: UART0_TX	011: IR1_TX
			100: Reserved	101: Reserved
26:24	R/W	0	110: Reserved	111: Reserved
23	/	/	Reserved	
			PB21_SELECT	
			000: Input	001: Output
			010: TWI2_SDA	011: Reserved
			100: Reserved	101: Reserved
22:20	R/W	0	110: Reserved	111: Reserved
19	/	/	/	
18:16	R/W	0	PB20_SELECT	

			000: Input 010: TWI2_SCK 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: Reserved
15	/	/	/	
14:12	R/W	0	PB19_SELECT 000: Input 010: TWI1_SDA 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PB18_SELECT 000: Input 010: TWI1_SCK 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PB17_SELECT 000: Input 010: SPI2_MISO 100: Reserved 110: Reserved	 001: Output 011: JTAG_DI0 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PB16_SELECT 000: Input 010: SPI2_MOSI 100: Reserved 110: Reserved	 001: Output 011: JTAG_DO0 101: Reserved 111: Reserved

3.13. PB Configure Register 3

Offset: 0x30			Register Name: PB_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.14. PB Data Register

Offset: 0x34			Register Name: PB_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/

23:0	R/W	0	PB_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.15. PB Multi-Driving Register 0

Offset: 0x38			Register Name: PB_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.16. PB Multi-Driving Register 1

Offset: 0x3C			Register Name: PB_DRV1 Default Value: 0x0000_5555
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 16~23) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.17. PB Pull Register 0

Offset: 0x40			Register Name: PB_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18. PB Pull Register 1

Offset: 0x44			Register Name: PB_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 16~23) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.19. PC Configure Register 0

Offset: 0x48			Register Name: PC_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PC7_SELECT 000: Input 001: Output 010: NRB1 011: SDC2_CLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PC6_SELECT 000: Input 001: Output 010: NRB0 011: SDC2_CMD 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PC5_SELECT 000: Input 001: Output 010: NRE# 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PC4_SELECT 000: Input 001: Output 010: NCE0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PC3_SELECT

			000: Input 010: NCE1 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PC2_SELECT 000: Input 010: NCLE 100: Reserved 110: Reserved	 001: Output 011: SPI0_CLK 101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PC1_SELECT 000: Input 010: NALE 100: Reserved 110: Reserved	 001: Output 011: SPI0_MISO 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PC0_SELECT 000: Input 010: NWE 100: Reserved 110: Reserved	 001: Output 011: SPI0_MOSI 101: Reserved 111: Reserved

3.20. PC Configure Register 1

Offset: 0x4C			**Register Name: PC_CFG1** **Default Value: 0x0000_0000**	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0	PC15_SELECT 000: Input 010: NDQ7 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: Reserved
27	/	/	/	
26:24	R/W	0	PC14_SELECT 000: Input 010: NDQ6 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: Reserved
23	/	/	/	
22:20	R/W	0	PC13_SELECT 000: Input	 001: Output

			010: NDQ5	011: Reserved
			100: Reserved	101: Reserved
			110: Reserved	111: Reserved
19	/	/	/	
			PC12_SELECT	
			000: Input	001: Output
			010: NDQ4	011: Reserved
			100: Reserved	101: Reserved
18:16	R/W	0	110: Reserved	111: Reserved
15	/	/	/	
			PC11_SELECT	
			000: Input	001: Output
			010: NDQ3	011: SDC2_D3
			100: Reserved	101: Reserved
14:12	R/W	0	110: Reserved	111: Reserved
11	/	/	/	
			PC10_SELECT	
			000: Input	001: Output
			010: NDQ2	011: SDC2_D2
			100: Reserved	101: Reserved
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
			PC9_SELECT	
			000: Input	001: Output
			010: NDQ1	011: SDC2_D1
			100: Reserved	101: Reserved
6:4	R/W	0	110: Reserved	111: Reserved
3	/	/	/	
			PC8_SELECT	
			000: Input	001: Output
			010: NDQ0	011: SDC2_D0
			100: Reserved	101: Reserved
2:0	R/W	0	110: Reserved	111: Reserved

3.21. PC Configure Register 2

Offset: 0x50			**Register Name: PC_CFG2** **Default Value: 0x0000_0000**	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
			PC23_SELECT	
			000: Input	001: Output
30:28	R/W	0	010: Reserved	011: SPI0_CS0

			100: Reserved	101: Reserved
			110: Reserved	111: Reserved
17	/	/	/	
			PC22_SELECT	
			000: Input	001: Output
			010: NCE7	011: SPI2_MISO
			100: Reserved	101: Reserved
26:24	R/W	0	110: Reserved	111: Reserved
23	/	/	/	
			PC21_SELECT	
			000: Input	001: Output
			010: NCE6	011: SPI2_MOSI
			100: Reserved	101: Reserved
22:20	R/W	0	110: Reserved	111: Reserved
19	/	/	/	
			PC20_SELECT	
			000: Input	001: Output
			010: NCE5	011: SPI2_CLK
			100: Reserved	101: Reserved
18:16	R/W	0	110: Reserved	111: Reserved
15	/	/	/	
			PC19_SELECT	
			000: Input	001: Output
			010: NCE4	011: SPI2_CS0
			100: Reserved	101: Reserved
14:12	R/W	0	110: Reserved	111: Reserved
11	/	/	/	
			PC18_SELECT	
			000: Input	001: Output
			010: NCE3	011: Reserved
			100: Reserved	101: Reserved
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
			PC17_SELECT	
			000: Input	001: Output
			010: NCE2	011: Reserved
			100: Reserved	101: Reserved
6:4	R/W	0	110: Reserved	111: Reserved
3	/	/	/	
			PC16_SELECT	
			000: Input	001: Output
			010: NWP	011: Reserved
2:0	R/W	0	100: Reserved	101: Reserved

			110: Reserved	111: Reserved

3.22. PC Configure Register 3

Offset: 0x54			Register Name: PC_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
3	/	/	/
2:0	R/W	0	PC24_SELECT 000: Input 001: Output 010: NDQS 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

3.23. PC Data Register

Offset: 0x58			Register Name: PC_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R/W	0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.24. PC Multi-Driving Register 0

Offset: 0x5C			Register Name: PC_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PC_DRV PC[n] Multi-Driving_SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.25. PC Multi-Driving Register 1

Offset: 0x60			Register Name: PC_DRV1 Default Value: 0x0001_5555
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
[2i+1:2i] (i=0~8)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 16~24) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.26. PC Pull Register 0

Offset: 0x64			Register Name: PC_PULL0 Default Value: 0x0000_5140
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0000_5140	PC_PULL PC[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.27. PC Pull Register 1

Offset: 0x68			Register Name: PC_PULL1 Default Value: 0x0000_4016
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
[2i+1:2i] (i=0~8)	R/W	0x0000_4016	PC_PULL PC[n] Pull-up/down Select (n = 16~24) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.28. PD Configure Register 0

Offset: 0x6C			Register Name: PD_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PD7_SELECT 000: Input 001: Output

			010: LCD0_D7	011: LVDS0_VNC
			100: Reserved	101: Reserved
			110: Reserved	111: Reserved
27	/	/	Reserved	
			PD6_SELECT	
			000: Input	001: Output
			010: LCD0_D6	011: LVDS0_VPC
			100: Reserved	101: Reserved
26:24	R/W	0	110: Reserved	111: Reserved
23	/	/	/	
			PD5_SELECT	
			000: Input	001: Output
			010: LCD0_D5	011: LVDS0_VN2
			100: Reserved	101: Reserved
22:20	R/W	0	110: Reserved	111: Reserved
19	/	/	/	
			PD4_SELECT	
			000: Input	001: Output
			010: LCD0_D4	011: LVDS0_VP2
			100: Reserved	101: Reserved
18:16	R/W	0	110: Reserved	111: Reserved
15	/	/	/	
			PD3_SELECT	
			000: Input	001: Output
			010: LCD0_D3	011: LVDS0_VN1
			100: Reserved	101: Reserved
14:12	R/W	0	110: Reserved	111: Reserved
11	/	/	/	
			PD2_SELECT	
			000: Input	001: Output
			010: LCD0_D2	011: LVDS0_VP1
			100: Reserved	101: Reserved
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
			PD1_SELECT	
			000: Input	001: Output
			010: LCD0_D1	011: LVDS0_VN0
			100: Reserved	101: Reserved
6:4	R/W	0	110: Reserved	111: Reserved
3	/	/	/	
			PD0_SELECT	
			000: Input	001: Output
2:0	R/W	0	010: LCD0_D0	011: LVDS0_VP0

			100: Reserved	101: Reserved
			110: Reserved	111: Reserved

3.29. PD Configure Register 1

Offset: 0x70			Register Name: PD_CFG1 Default Value: 0x0000_0000	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0	PD15_SELECT 000: Input 010: LCD0_D15 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VN2 101: Reserved 111: Reserved
27	/	/	/	
26:24	R/W	0	PD14_SELECT 000: Input 010: LCD0_D14 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VP2 101: Reserved 111: Reserved
23	/	/	/	
22:20	R/W	0	PD13_SELECT 000: Input 010: LCD0_D13 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VN1 101: Reserved 111: Reserved
19	/	/	/	
18:16	R/W	0	PD12_SELECT 000: Input 010: LCD0_D12 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VP1 101: Reserved 111: Reserved
15	/	/	/	
14:12	R/W	0	PD11_SELECT 000: Input 010: LCD0_D11 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VN0 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PD10_SELECT 000: Input 010: LCD0_D10	 001: Output 011: LVDS1_VP0

			100: Reserved 110: Reserved	101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PD9_SELECT 000: Input 010: LCD0_D9 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VM3 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PD8_SELECT 000: Input 010: LCD0_D8 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP3 101: Reserved 111: Reserved

3.30. PD Configure Register 2

Offset: 0x74			Register Name: PD_CFG2 Default Value: 0x0000_0000	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0	PD23_SELECT 000: Input 010: LCD0_D23 100: Reserved 110: Reserved	 001: Output 011: SMC_DET 101: Reserved 111: Reserved
27	/	/	/	
26:24	R/W	0	PD22_SELECT 000: Input 010: LCD0_D22 100: Reserved 110: Reserved	 001: Output 011: SMC_VPPPP 101: Reserved 111: Reserved
23	/	/	/	
22:20	R/W	0	PD21_SELECT 000: Input 010: LCD0_D21 100: Reserved 110: Reserved	 001: Output 011: SMC_VPPEN 101: Reserved 111: Reserved
19	/	/	/	
18:16	R/W	0	PD20_SELECT 000: Input 010: LCD0_D20 100: Reserved	 001: Output 011: CSI1_MCLK 101: Reserved

			110: Reserved	111: Reserved
15	/	/	/	
14:12	R/W	0	PD19_SELECT 000: Input 010: LCD0_D19 100: Reserved 110: Reserved	001: Output 011: LVDS1_VN3 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PD18_SELECT 000: Input 010: LCD0_D18 100: Reserved 110: Reserved	001: Output 011: LVDS1_VP3 101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PD17_SELECT 000: Input 010: LCD0_D17 100: Reserved 110: Reserved	001: Output 011: LVDS1_VNC 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PD16_SELECT 000: Input 010: LCD0_D16 100: Reserved 110: Reserved	001: Output 011: LVDS1_VPC 101: Reserved 111: Reserved

3.31. PD Configure Register 3

Offset: 0x78			**Register Name: PD_CFG3** **Default Value: 0x0000_0000**	
Bit	**Read/Write**	**Default**	**Description**	
31:16	/	/	/	
15	/	/	/	
14:12	R/W	0	PD27_SELECT 000: Input 010: LCD0_ VSYNC 100: Reserved 110: Reserved	001: Output 011: SMC_SDA 101: Reserved 111: Reserved
11	/	/	Reserved	
10:8	R/W	0	PD26_SELECT 000: Input 010: LCD0_ HSYNC	001: Output 011: SMC_SCK

			100: Reserved 110: Reserved	101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PD25_SELECT 000: Input 010: LCD0_ DE 100: Reserved 110: Reserved	 001: Output 011: SMC_RST 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PD24_SELECT 000: Input 010: LCD0_CLK 100: Reserved 110: Reserved	 001: Output 011: SMC_VCCEN 101: Reserved 111: Reserved

3.32. PD Data Register

Offset: 0x7C			Register Name: PD_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.33. PD Multi-Driving Register 0

Offset: 0x80			Register Name: PD_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.34. PD Multi-Driving Register 1

Offset: 0x84			Register Name: PD_DRV1 Default Value: 0x0055_5555
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.35. PD Pull Register 0

Offset: 0x88			Register Name: PD_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.36. PD Pull Register 1

Offset: 0x8C			Register Name: PD_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.37. PE Configure Register 0

Offset: 0x90			Register Name: PE_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PE7_SELECT 000: Input 001: Output

			010: TS0_D3	011: CSI0_D3
			100: Reserved	101: Reserved
			110: Reserved	111: Reserved
27	/	/	/	
			PE6_SELECT	
			000: Input	001: Output
			010: TS0_D2	011: CSI0_D2
			100: Reserved	101: Reserved
26:24	R/W	0	110: Reserved	111: Reserved
23	/	/	/	
			PE5_SELECT	
			000: Input	001: Output
			010: TS0_D1	011: CSI0_D1
			100: SMC_VPPEN	101: Reserved
22:20	R/W	0	110: Reserved	111: Reserved
19	/	/	/	
			PE4_SELECT	
			000: Input	001: Output
			010: TS0_D0	011: CSI0_D0
			100: Reserved	101: Reserved
18:16	R/W	0	110: Reserved	111: Reserved
15	/	/	/	
			PE3_SELECT	
			000: Input	001: Output
			010: TS0_DVLD	011: CSI0_VSYNC
			100: Reserved	101: Reserved
14:12	R/W	0	110: Reserved	111: Reserved
11	/	/	/	
			PE2_SELECT	
			000: Input	001: Output
			010: TS0_SYNC	011: CSI0_HSYNC
			100: Reserved	101: Reserved
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
			PE1_SELECT	
			000: Input	001: Output
			010: TS0_ERR	011: CSI0_CK
			100: Reserved	101: Reserved
6:4	R/W	0	110: Reserved	111: Reserved
3	/	/	/	
			PE0_SELECT	
			000: Input	001: Output
2:0	R/W	0	010: TS0_CLK	011: CSI0_PCK

			100: Reserved	101: Reserved
			110: Reserved	111: Reserved

3.38. PE Configure Register 1

Offset: 0x94			Register Name: PE_CFG1 Default Value: 0x0000_0000	
Bit	**Read/Write**	**Default**	**Description**	
31:16	/	/	/	
15	/	/	/	
14:12	R/W	0	PE11_SELECT 000: Input 010: TS0_D7 100: Reserved 110: Reserved	001: Output 011: CSI0_D7 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PE10_SELECT 000: Input 010: TS0_D6 100: Reserved 110: Reserved	001: Output 011: CSI0_D6 101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PE9_SELECT 000: Input 010: TS0_D5 100: Reserved 110: Reserved	001: Output 011: CSI0_D5 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PE8_SELECT 000: Input 010: TS0_D4 100: Reserved 110: Reserved	001: Output 011: CSI0_D4 101: Reserved 111: Reserved

3.39. PE Configure Register 2

Offset: 0x98			Register Name: PE_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.40. PE Configure Register 3

Offset: 0x98			Register Name: PE_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.41. PE Data Register

Offset: 0xA0			Register Name: PE_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11:0	R/W	0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.42. PE Multi-Driving Register 0

Offset: 0xA4			Register Name: PE_DRV0 Default Value: 0x0055_5555
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PE_DRV PE[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.43. PE Multi-Driving Register 1

Offset: 0xA8			Register Name: PE_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.44. PE Pull Register 0

Offset: 0xAC			Register Name: PE_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.45. PE Pull Register 1

Offset: 0xB0			Register Name: PE_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.46. PF Configure Register 0

Offset: 0xB4			Register Name: PF_CFG0 Default Value: 0x0040_4044
Bit	**Read/Write**	**Default**	**Description**
31:23	/	/	/
22:20	R/W	0x4	PF5_SELECT 000: Input 001: Output 010: SDC0_D2 011: Reserved 100: JTAG_CK1 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PF4_SELECT 000: Input 001: Output 010: SDC0_D3 011: Reserved 100: UART0_RX 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0x4	PF3_SELECT 000: Input 001: Output 010: SDC0_CMD 011: Reserved 100: JTAG_DO1 101: Reserved 110: Reserved 111: Reserved

11	/	/	/
10:8	R/W	0	PF2_SELECT 000: Input 001: Output 010: SDC0_CLK 011: Reserved 100: UART0_TX 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0x4	PF1_SELECT 000: Input 001: Output 010: SDC0_D0 011: Reserved 100: JTAG_DI1 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0x4	PF0_SELECT 000: Input 001: Output 010: SDC0_D1 011: Reserved 100: JTAG_MS1 101: Reserved 110: Reserved 111: Reserved

3.47. PF Configure Register 1

Offset: 0xB8			Register Name: PF_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.48. PF Configure Register 2

Offset: 0xBC			Register Name: PF_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.49. PF Configure Register 3

Offset: 0xC0			Register Name: PF_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.50. PF Data Register

Offset: 0xC4			Register Name: PF_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5:0	R/W	0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.51. PF Multi-Driving Register 0

Offset: 0xC8			Register Name: PF_DRV0 Default Value: 0x0000_0555
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x1	PF_DRV PF[n] Multi-Driving Select (n = 0~5) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.52. PF Multi-Driving Register 1

Offset: 0xCC			Register Name: PF_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/

3.53. PF Pull Register 0

Offset: 0xD0			Register Name: PF_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~5)

			00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved

3.54. PF Pull Register 1

Offset: 0xD4			Register Name: PF_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.55. PG Configure Register 0

Offset: 0xD8			Register Name: PG_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PG7_SELECT 000: Input 001: Output 010: TS1_D3 011: CSI1_D3 100: UART3_RX 101: CSI0_D11 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PG6_SELECT 000: Input 001: Output 010: TS1_D2 011: CSI1_D2 100: UART3_TX 101: CSI0_D10 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PG5_SELECT 000: Input 001: Output 010: TS1_D1 011: CSI1_D1 100: SDC1_D3 101: CSI0_D9 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PG4_SELECT 000: Input 001: Output 010: TS1_D0 011: CSI1_D0 100: SDC1_D2 101: CSI0_D8 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PG3_SELECT 000: Input 001: Output

			010: TS1_DVLD	011: CSI1_VSYNC
			100: SDC1_D1	101: Reserved
			110: Reserved	111: Reserved
11	/	/	/	
			PG2_SELECT	
			000: Input	001: Output
			010: TS1_SYNC	011: CSI1_HSYNC
			100: SDC1_D0	101: Reserved
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
			PG1_SELECT	
			000: Input	001: Output
			010: TS1_ERR	011: CSI1_CK
			100: SDC1_CLK	101: Reserved
6:4	R/W	0	110: Reserved	111: Reserved
3	/	/	/	
			PG0_SELECT	
			000: Input	001: Output
			010: TS1_CLK	011: CSI1_PCK
			100: SDC1_CMD	101: Reserved
2:0	R/W	0	110: Reserved	111: Reserved

3.56. PG Configure Register 1

Offset: 0xDC			**Register Name: PG_CFG1** **Default Value: 0x0000_0000**	
Bit	**Read/Write**	**Default**	**Description**	
31:7	/	/	/	
15	/	/	/	
			PG11_SELECT	
			000: Input	001: Output
			010: TS1_D7	011: CSI1_D7
			100: UART4_RX	101: CSI0_D15
14:12	R/W	0	110: Reserved	111: Reserved
11	/	/	/	
			PG10_SELECT	
			000: Input	001: Output
			010: TS1_D6	011: CSI1_D6
			100: UART4_TX	101: CSI0_D14
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
6:4	R/W	0	PG9_SELECT	

			000: Input 010: TS1_D5 100: UART3_CTS 110: Reserved	001: Output 011: CSI1_D5 101: CSI0_D13 111: Reserved
3	/	/	/	
2:0	R/W	0	PG8_SELECT 000: Input 010: TS1_D4 100: UART3_RTS 110: Reserved	 001: Output 011: CSI1_D4 101: CSI0_D12 111: Reserved

3.57. PG Configure Register 2

Offset: 0xE0			Register Name: PG_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.58. PG Configure Register 3

Offset: 0xE4			Register Name: PG_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.59. PG Data Register

Offset: 0xE8			Register Name: PG_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11:0	R/W	0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.60. PG Multi-Driving Register 0

Offset: 0xEC			Register Name: PG_DRV0 Default Value: 0x0555_5555
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PG_DRV PG[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.61. PG Multi-Driving Register 1

Offset: 0xF0			Register Name: PG_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/

3.62. PG Pull Register 0

Offset: 0xF4			Register Name: PG_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.63. PG Pull Register 1

Offset: 0xF8			Register Name: PG_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.64. PH Configure Register 0

Offset: 0xFC	Register Name: PH_CFG0

			Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PH7_SELECT 000: Input 001: Output 010: LCD1_D7 011: ATAD3 100: UART5_RX 101: MS_CLK 110: EINT7 111: CSI1_D7
27	/	/	/
26:24	R/W	0	PH6_SELECT 000: Input 001: Output 010: LCD1_D6 011: ATAD2 100: UART5_TX 101: MS_BS 110: EINT6 111: CSI1_D6
23	/	/	/
22:20	R/W	0	PH5_SELECT 000: Input 001: Output 010: LCD1_D5 011: ATAD1 100: UART4_RX 101: Reserved 110: EINT5 111: CSI1_D5
19	/	/	/
18:16	R/W	0	PH4_SELECT 000: Input 001: Output 010: LCD1_D4 011: ATAD0 100: UART4_TX 101: Reserved 110: EINT4 111: CSI1_D4
15	/	/	/
14:12	R/W	0	PH3_SELECT 000: Input 001: Output 010: LCD1_D3 011: ATAIRQ 100: UART3_CTS 101: Reserved 110: EINT3 111: CSI1_D3
11	/	/	/
10:8	R/W	0	PH2_SELECT 000: Input 001: Output 010: LCD1_D2 011: ATAA2 100: UART3_RTS 101: Reserved 110: EINT2 111: CSI1_D2
7	/	/	/
6:4	R/W	0	PH1_SELECT 000: Input 001: Output 010: LCD1_D1 011: ATAA1 100: UART3_RX 101: Reserved

			110: EINT1	111: CSI1_D1
3	/	/	/	
2:0	R/W	0	PH0_SELECT 000: Input 010: LCD1_D0 100: UART3_TX 110: EINT0	001: Output 011: ATAA0 101: Reserved 111: CSI1_D0

3.65. PH Configure Register 1

Offset: 0x100			Register Name: PH_CFG1 Default Value: 0x0000_0000	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0	PH15_SELECT 000: Input 010: LCD1_D15 100: KP_IN5 110: EINT15	001: Output 011: ATAD11 101: SMC_VPPPP 111: CSI1_D15
27	/	/	/	
26:24	R/W	0	PH14_SELECT 000: Input 010: LCD1_D14 100: KP_IN4 110: EINT14	001: Output 011: ATAD10 101: SMC_VPPEN 111: CSI1_D14
23	/	/	/	
22:20	R/W	0	PH13_SELECT 000: Input 010: LCD1_D13 100: PS2_SDA1 110: EINT13	001: Output 011: ATAD9 101: SMC_RST 111: CSI1_D13
19	/	/	/	
18:16	R/W	0	PH12_SELECT 000: Input 010: LCD1_D12 100: PS2_SCK1 110: EINT12	001: Output 011: ATAD8 101: Reserved 111: CSI1_D12
15	/	/	/	
14:12	R/W	0	PH11_SELECT 000: Input 010: LCD1_D11 100: KP_IN3 110: EINT11	001: Output 011: ATAD7 101: MS_D3 111: CSI1_D11

11	/	/	/
10:8	R/W	0	PH10_SELECT 000: Input 001: Output 010: LCD1_D10 011: ATAD6 100: KP_IN2 101: MS_D2 110: EINT10 111: CSI1_D10
7	/	/	/
6:4	R/W	0	PH9_SELECT 000: Input 001: Output 010: LCD1_D9 011: ATAD5 100: KP_IN1 101: MS_D1 110: EINT9 111: CSI1_D9
3	/	/	/
2:0	R/W	0	PH8_SELECT 000: Input 001: Output 010: LCD1_D8 011: ATAD4 100: KP_IN0 101: MS_D0 110: EINT8 111: CSI1_D8

3.66. PH Configure Register 2

Offset: 0x104			**Register Name: PH_CFG2** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PH23_SELECT 000: Input 001: Output 010: LCD1_D23 011: ATACS0 100: KP_OUT3 101: SDC1_CLK 110: Reserved 111: CSI1_D23
27	/	/	/
26:24	R/W	0	PH22_SELECT 000: Input 001: Output 010: LCD1_D22 011: ATADACK 100: KP_OUT2 101: SDC1_CMD 110: Reserved 111: CSI1_D22
23	/	/	/
22:20	R/W	0	PH21_SELECT 000: Input 001: Output 010: LCD1_D21 011: ATADREQ 100: CAN_RX 101: Reserved 110: EINT21 111: CSI1_D21
19	/	/	/

			PH20_SELECT	
			000: Input	001: Output
			010: LCD1_D20	011: ATAOE
			100: CAN_TX	101: Reserved
18:16	R/W	0	110: EINT20	111: CSI1_D20
15	/	/	/	
			PH19_SELECT	
			000: Input	001: Output
			010: LCD1_D19	011: ATAD15
			100: KP_OUT1	101: SMC_SDA
14:12	R/W	0	110: EINT19	111: CSI1_D19
11	/	/	/	
			PH18_SELECT	
			000: Input	001: Output
			010: LCD1_D18	011: ATAD14
			100: KP_OUT0	101: SMC_SCK
10:8	R/W	0	110: EINT18	111: CSI1_D18
7	/	/	/	
			PH17_SELECT	
			000: Input	001: Output
			010: LCD1_D17	011: ATAD13
			100: KP_IN7	101: SMC_VCCEN
6:4	R/W	0	110: EINT17	111: CSI1_D17
3	/	/	/	
			PH16_SELECT	
			000: Input	001: Output
			010: LCD1_D16	011: ATAD12
			100: KP_IN6	101: Reserved
2:0	R/W	0	110: EINT16	111: CSI1_D16

3.67. PH Configure Register 3

Offset: 0x108			**Register Name: PH_CFG3** **Default Value: 0x0000_0000**	
Bit	**Read/Write**	**Default**	**Description**	
31:16	/	/	/	
15	/	/	/	
			PH27_SELECT	
			000: Input	001: Output
			010: LCD1_ VSYNC	011: ATAIOW
			100: KP_OUT7	101: SDC1_D3
14:12	R/W	0	110: Reserved	111: CSI1_VSYNC
11	/	/	Reserved	

10:8	R/W	0	PH26Select 000: Input 001: Output 010: LCD1_HSYNC 011: ATAIOR 100: KP_OUT6 101: SDC1_D2 110: Reserved 111: CSI1_HSYNC
7	/	/	/
6:4	R/W	0	PH25_SELECT 000: Input 001: Output 010: LCD1_DE 011: ATAIORDY 100: KP_OUT5 101: SDC1_D1 110: Reserved 111: CSI1_FIELD
3	/	/	/
2:0	R/W	0	PH24_SELECT 000: Input 001: Output 010: LCD1_CLK 011: ATACS1 100: KP_OUT4 101: SDC1_D0 110: Reserved 111: CSI1_PCLK

3.68. PH Data Register

Offset: 0x10C			**Register Name: PH_DAT** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.69. PH Multi-Driving Register 0

Offset: 0x110			**Register Name: PH_DRV0** **Default Value: 0x5555_5555**
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.70. PH Multi-Driving Register 1

Offset: 0x114			Register Name: PH_DRV1 Default Value: 0x0055_5555
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.71. PH Pull Register 0

Offset: 0x118			Register Name: PH_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PH_PULL PH[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.72. PH Pull Register 1

Offset: 0x11C			Register Name: PH_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PH_PULL PH[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.73. PI Configure Register 0

Offset: 0x120			Register Name: PI_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PI7_SELECT 000: Input 001: Output

			010: SDC3_D1	011: Reserved
			100: Reserved	101: Reserved
			110: Reserved	111: Reserved
27	/	/	/	
			PI6_SELECT	
			000: Input	001: Output
			010: SDC3_D0	011: Reserved
			100: Reserved	101: Reserved
26:24	R/W	0	110: Reserved	111: Reserved
23	/	/	/	
			PI5_SELECT	
			000: Input	001: Output
			010: SDC3_CLK	011: Reserved
			100: Reserved	101: Reserved
22:20	R/W	0	110: Reserved	111: Reserved
19	/	/	/	
			PI4_SELECT	
			000: Input	001: Output
			010: SDC3_CMD	011: Reserved
			100: Reserved	101: Reserved
18:16	R/W	0	110: Reserved	111: Reserved
15	/	/	/	
			PI3_SELECT	
			000: Input	001: Output
			010: PWM1	011: Reserved
			100: Reserved	101: Reserved
14:12	R/W	0	110: Reserved	111: Reserved
11	/	/	/	
			PI2_SELECT	
			000: Input	001: Output
			010: Reserved	011: Reserved
			100: Reserved	101: Reserved
10:8	R/W	0	110: Reserved	111: Reserved
7	/	/	/	
			PI1_SELECT	
			000: Input	001: Output
			010: Reserved	011: Reserved
			100: Reserved	101: Reserved
6:4	R/W	0	110: Reserved	111: Reserved
3	/	/	/	
			PI0_SELECT	
			000: Input	001: Output
2:0	R/W	0	010: Reserved	011: Reserved

			100: Reserved	101: Reserved
			110: Reserved	111: Reserved

3.74. PI Configure Register 1

Offset: 0x124			Register Name: PI_CFG1 Default Value: 0x0000_0000	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0	PI15_SELECT 000: Input 010: SPI1_CS1 100: TCLKIN1 110: EINT27	001: Output 011: PS2_SDA1 101: Reserved 111: Reserved
27	/	/	/	
26:24	R/W	0	PI14_SELECT 000: Input 010: SPI0_CS1 100: TCLKIN0 110: EINT26	001: Output 011: PS2_SCK1 101: Reserved 111: Reserved
23	/	/	/	
22:20	R/W	0	PI13_SELECT 000: Input 010: SPI0_MISO 100: Reserved 110: EINT25	001: Output 011: UART6_RX 101: Reserved 111: Reserved
19	/	/	/	
18:16	R/W	0	PI12_SELECT 000: Input 010: SPI0_MOSI 100: Reserved 110: EINT24	001: Output 011: UART6_TX 101: Reserved 111: Reserved
15	/	/	/	
14:12	R/W	0	PI11_SELECT 000: Input 010: SPI0_CLK 100: Reserved 110: EINT23	001: Output 011: UART5_RX 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PI10_SELECT 000: Input 010: SPI0_CS0 100: Reserved	001: Output 011: UART5_TX 101: Reserved

			110: EINT22	111: Reserved
7	/	/	/	
6:4	R/W	0	PI9_SELECT 000: Input 010: SDC3_D3 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PI8_SELECT 000: Input 010: SDC3_D2 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: Reserved

3.75. PI Configure Register 2

Offset: 0x128			Register Name: PI_CFG2 Default Value: 0x0000_0000	
Bit	**Read/Write**	**Default**	**Description**	
31:24	/	/	/	
23	/	/	/	
22:20	R/W	0	PI21_SELECT 000: Input 010: PS2_SDA0 100: HSDA 110: Reserved	001: Output 011: UART7_RX 101: Reserved 111: Reserved
19	/	/	/	
18:16	R/W	0	PI20_SELECT 000: Input 010: PS2_SCK0 100: HSCL 110: Reserved	001: Output 011: UART7_TX 101: Reserved 111: Reserved
15	/	/	/	
14:12	R/W	0	PI19_SELECT 000: Input 010: SPI1_MISO 100: Reserved 110: EINT31	001: Output 011: UART2_RX 101: Reserved 111: Reserved
11	/	/	/	
10:8	R/W	0	PI18_SELECT 000: Input 010: SPI1_MOSI	001: Output 011: UART2_TX

			100: Reserved 110: EINT30	101: Reserved 111: Reserved
7	/	/	/	
6:4	R/W	0	PI17_SELECT 000: Input 010: SPI1_CLK 100: Reserved 110: EINT29	001: Output 011: UART2_CTS 101: Reserved 111: Reserved
3	/	/	/	
2:0	R/W	0	PI16_SELECT 000: Input 010: SPI1_CS0 100: Reserved 110: EINT28	001: Output 011: UART2_RTS 101: Reserved 111: Reserved

3.76. PI Configure Register 3

Offset: 0x12C			Register Name: PI_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.77. PI Data Register

Offset: 0x130			Register Name: PI_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:13	/	/	/
12:0	R/W	0	PI_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.78. PI Multi-Driving Register 0

Offset: 0x134			Register Name: PI_DRV0 Default Value: 0x0155_5555
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/

[2i+1:2i] (i=0~12)	R/W	0x1	PI_DRV PI[n] Multi-Driving Select (n = 0~12) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.79. PI Multi-Driving Register 1

Offset: 0x138			Register Name: PI_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.80. PI Pull Register 0

Offset: 0x13C			Register Name: PI_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
[2i+1:2i] (i=0~12)	R/W	0x0	PI_PULL PI[n] Pull-up/down Select (n = 0~12) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.81. PI Pull Register 1

Offset: 0x140			Register Name: PI_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.82. PIO Interrupt Configure Register 0

Offset: 0x200			Register Name: PIO_INT_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level

			0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.83. PIO Interrupt Configure Register 1

Offset: 0x204			Register Name: PIO_INT_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 8~15) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.84. PIO Interrupt Configure Register 2

Offset: 0x208			Register Name: PIO_INT_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 16~23) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.85. PIO Interrupt Configure Register 3

Offset: 0x20C			Register Name: PIO_INT_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	PIO_INT_CFG External INTn Mode (n = 24~31) 0x0: Positive Edge 0x1: Negative Edge

			0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.86. PIO Interrupt Control Register

Offset: 0x210			Register Name: PIO_INT_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[n] (n=0~31)	R/W	0	PIO_INT_CTL External INTn Enable (n = 0~31) 0: Disable 1: Enable

3.87. PIO Interrupt Status Register

Offset: 0x214			Register Name: PIO_INT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[n] (n=0~31)	R/W	0	PIO_INT_STATUS External INTn Pending Bit (n = 0~31) 0: No IRQ pending 1: IRQ pending Write '1' to clear

3.88. PIO Interrupt Debounce Register

Offset: 0x218			Register Name: PIO_INT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

4. Declaration

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