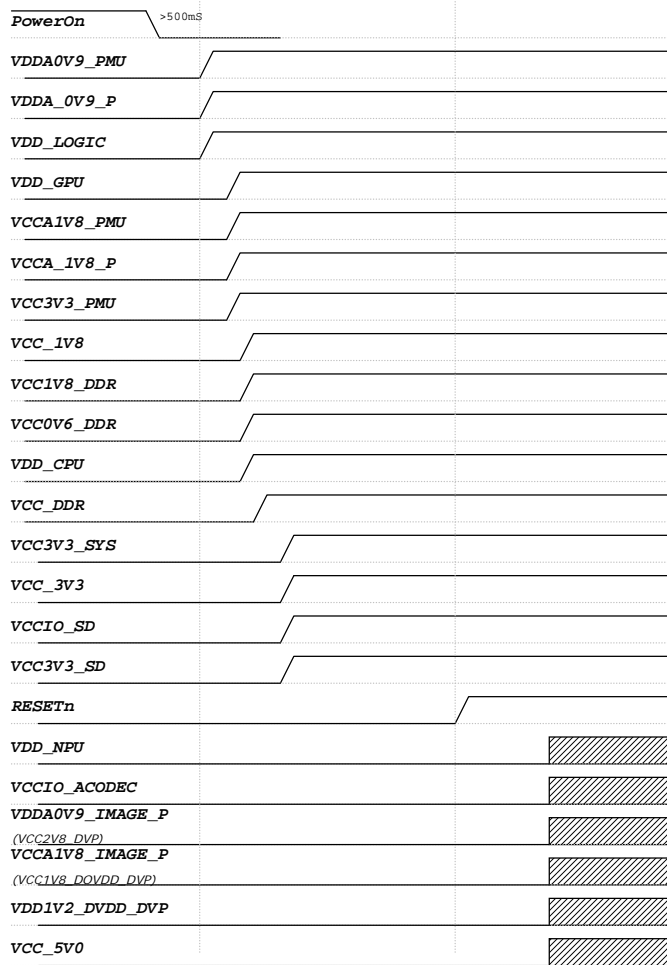




# Power Sequence(Use RK809-5)



# Power description(Use RK809-5)

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC_SYSIN	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC_SYSIN	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC_SYSIN	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC_SYSIN	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC_SYSIN	RK809_LDO1	0.4A	VDDA0V9_IMAGE_P (VCC2V8_DVP)	N/A	0V	OFF	2.8V (Camera)	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_P	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC_SYSIN	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (500 0-1.3V 500 0-1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_P	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC_SYSIN	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_P	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE_P (VCC1V8_D0VDD_DVP)	N/A	0V	OFF	1.8V (Camera)	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC_SYSIN	RK809_SW1 90mohm	2.1A	N/A						
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC_SYSIN	EXT BUCK	5.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC_SYSIN	EXT LDO	0.3A	VCC1V8_DDR	Slot:2A	1.8V	ON	1.8V	TBD	TBD
VCC_SYSIN	EXT BUCK	2.0A	VCC0V6_DDR	Slot:2A	0.6V	ON	0.6V	TBD	TBD
VCC3V3_SYS	EXT MOS		VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC_SYSIN	EXT LDO or BUCK	0.5A /1.0A	VDD1V2_DVDD_DVP	N/A	0V	OFF	1.2V (Camera)	TBD	TBD
VCC_SYSIN	EX BOOST	1.5A	VCC_5V0	N/A	0V	OFF	5.0V	TBD	TBD

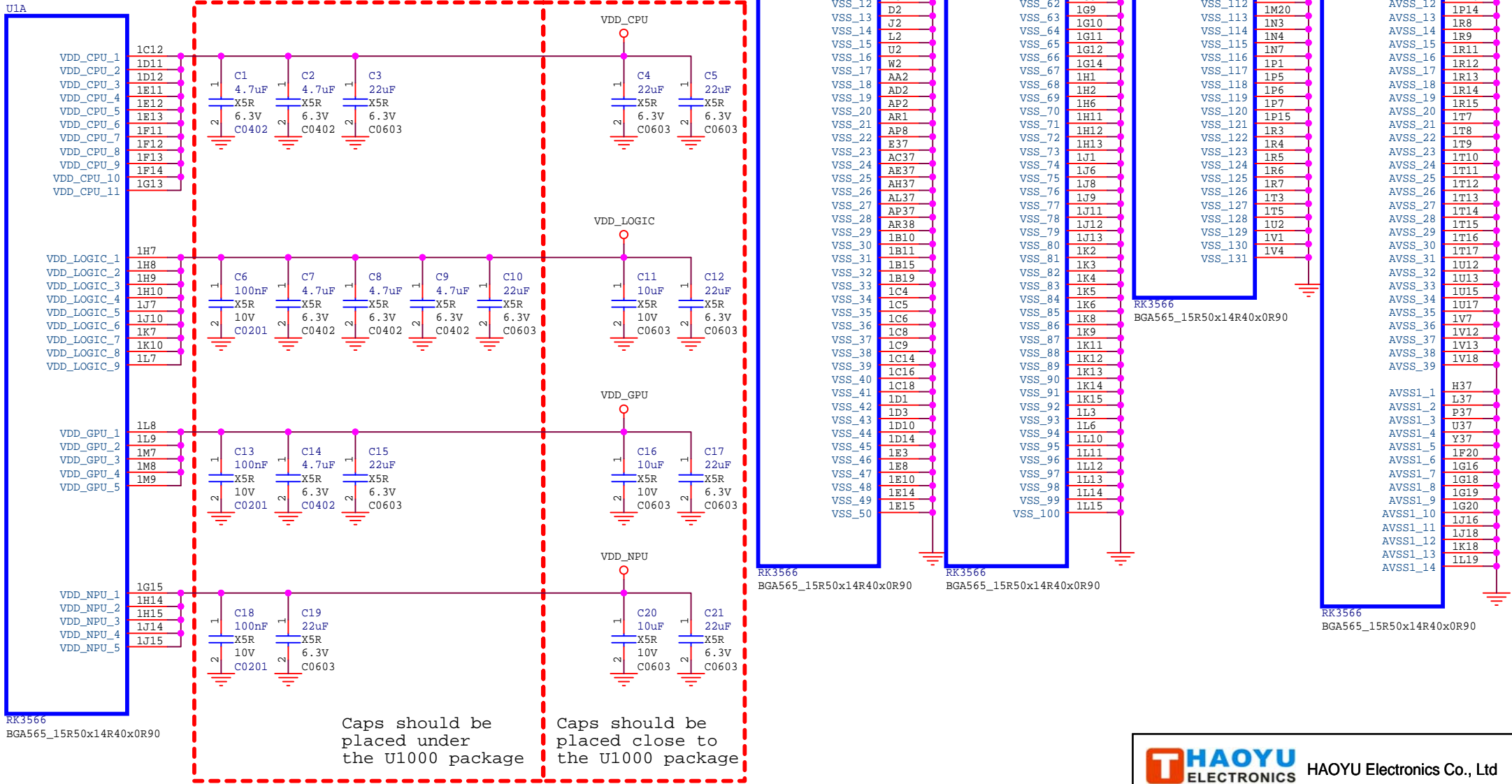
Check the software configuration(dts)  
of voltage level, which must be  
keep the same as hardware design

**!!! Attention**

<b>HAOYU</b> ELECTRONICS		HAOYU Electronics Co., Ltd	
Project:	MarsBoard_CM4_SODIMM		
File:	01.Power_Sequence/IO_Domain_Map		
Date:	Friday, November 04, 2022	Rev:	V1.0
Designed by:	Thomas	Reviewed by:	Thomas
		Sheet:	2 of 20

# RK3566\_ABCDE

## (Power&GND)



**HAOYU ELECTRONICS** HAOYU Electronics Co., Ltd

<b>Project:</b>	MarsBoard_CM4_SODIMM		
<b>File:</b>	02.RK3566_Power/GND		
<b>Date:</b>	Friday, November 04, 2022	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Thomas	<b>Reviewed by:</b>	Thomas
		<b>Sheet:</b>	3 of 20

# RK3566\_F(DDR PHY)

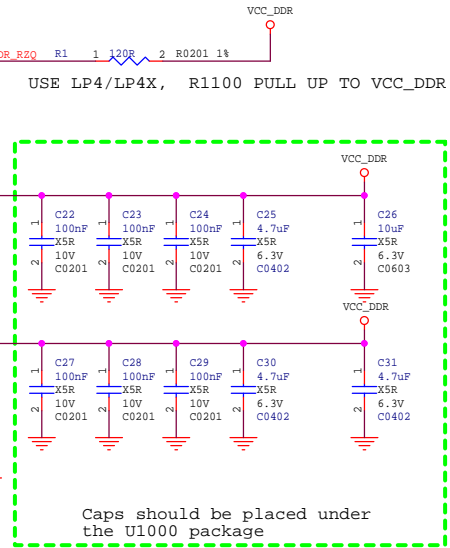
U1F

	DDR4	LPDDR4	DDR3	LPDDR3
26 LPDDR4_DQ0_A	DDR_DQ0_A G2	DDR_DQ0_A / DDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15
26 LPDDR4_DQ1_A	DDR_DQ1_A F2	DDR4_DQ1_A / DDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14
26 LPDDR4_DQ2_A	DDR_DQ2_A F1	DDR4_DQ2_A / DDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ13
26 LPDDR4_DQ3_A	DDR_DQ3_A E1	DDR4_DQ3_A / DDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ12
26 LPDDR4_DQ4_A	DDR_DQ4_A M2	DDR4_DQ4_A / DDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ11
26 LPDDR4_DQ5_A	DDR_DQ5_A K1	DDR4_DQ5_A / DDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ10
26 LPDDR4_DQ6_A	DDR_DQ6_A K2	DDR4_DQ6_A / DDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ9
26 LPDDR4_DQ7_A	DDR_DQ7_A 1E1	DDR4_DQ7_A / DDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ8
26 LPDDR4_DM0_A	DDR_DM0_A 1E2	DDR4_DML_A / LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
26 LPDDR4_DQS0P_A	DDR_DQS0P_A H2	DDR_DQS0P_A / DDR4_DQSL_P_A	DDR3_DQS0P	LPDDR3_DQS1P
26 LPDDR4_DQS0N_A	DDR_DQS0N_A H1	DDR_DQS0N_A / DDR4_DQSL_N_A	DDR3_DQS0N	LPDDR3_DQS1N
26 LPDDR4_DQ8_A	DDR_DQ8_A P2	DDR_DQ8_A / DDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25
26 LPDDR4_DQ9_A	DDR_DQ9_A R1	DDR_DQ9_A / DDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24
26 LPDDR4_DQ10_A	DDR_DQ10_A R2	DDR_DQ10_A / DDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ23
26 LPDDR4_DQ11_A	DDR_DQ11_A T2	DDR_DQ11_A / DDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ22
26 LPDDR4_DQ12_A	DDR_DQ12_A M1	DDR_DQ12_A / DDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ21
26 LPDDR4_DQ13_A	DDR_DQ13_A 1F2	DDR_DQ13_A / DDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ20
26 LPDDR4_DQ14_A	DDR_DQ14_A 1F1	DDR_DQ14_A / DDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ19
26 LPDDR4_DQ15_A	DDR_DQ15_A 1G2	DDR_DQ15_A / DDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ18
26 LPDDR4_DM1_A	DDR_DM1_A 1G1	DDR_DM1_A / DDR4_DML_A	DDR3_DM1	LPDDR3_DM3
26 LPDDR4_DQS1P_A	DDR_DQS1P_A N1	DDR_DQS1P_A / DDR4_DQSL_P_A	DDR3_DQS1P	LPDDR3_DQS1P
26 LPDDR4_DQS1N_A	DDR_DQS1N_A N2	DDR_DQS1N_A / DDR4_DQSL_N_A	DDR3_DQS1N	LPDDR3_DQS1N
26 LPDDR4_DQ0_B	DDR_DQ0_B B12	DDR_DQ0_B / DDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1
26 LPDDR4_DQ1_B	DDR_DQ1_B B10	DDR_DQ1_B / DDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ2
26 LPDDR4_DQ2_B	DDR_DQ2_B 1A8	DDR_DQ2_B / DDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ3
26 LPDDR4_DQ3_B	DDR_DQ3_B 1A7	DDR_DQ3_B / DDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4
26 LPDDR4_DQ4_B	DDR_DQ4_B B13	DDR_DQ4_B / DDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ5
26 LPDDR4_DQ5_B	DDR_DQ5_B 1A10	DDR_DQ5_B / DDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ6
26 LPDDR4_DQ6_B	DDR_DQ6_B 1B9	DDR_DQ6_B / DDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7
26 LPDDR4_DQ7_B	DDR_DQ7_B 1A9	DDR_DQ7_B / DDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ8
26 LPDDR4_DM0_B	DDR_DM0_B 1B8	DDR_DM0_B / DDR4_DML_B	DDR3_DM2	LPDDR3_DM0
26 LPDDR4_DQS0P_B	DDR_DQS0P_B A13	DDR_DQS0P_B / DDR4_DQSL_P_B	DDR3_DQS2P	LPDDR3_DQS0P
26 LPDDR4_DQS0N_B	DDR_DQS0N_B A12	DDR_DQS0N_B / DDR4_DQSL_N_B	DDR3_DQS2N	LPDDR3_DQS0N
26 LPDDR4_DQ8_B	DDR_DQ8_B B19	DDR_DQ8_B / DDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18
26 LPDDR4_DQ9_B	DDR_DQ9_B A19	DDR_DQ9_B / DDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19
26 LPDDR4_DQ10_B	DDR_DQ10_B A20	DDR_DQ10_B / DDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ20
26 LPDDR4_DQ11_B	DDR_DQ11_B B20	DDR_DQ11_B / DDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ21
26 LPDDR4_DQ12_B	DDR_DQ12_B B15	DDR_DQ12_B / DDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ22
26 LPDDR4_DQ13_B	DDR_DQ13_B C10	DDR_DQ13_B / DDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ23
26 LPDDR4_DQ14_B	DDR_DQ14_B C10	DDR_DQ14_B / DDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ24
26 LPDDR4_DQ15_B	DDR_DQ15_B B16	DDR_DQ15_B / DDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ25
26 LPDDR4_DM1_B	DDR_DM1_B 1A11	DDR_DM1_B / DDR4_DML_B	DDR3_DM3	LPDDR3_DM2
26 LPDDR4_DQS1P_B	DDR_DQS1P_B A17	DDR_DQS1P_B / DDR4_DQSL_P_B	DDR3_DQS3P	LPDDR3_DQS2P
26 LPDDR4_DQS1N_B	DDR_DQS1N_B B17	DDR_DQS1N_B / DDR4_DQSL_N_B	DDR3_DQS3N	LPDDR3_DQS2N

Note:  
Except DDR3, other DQ sequences  
can not be swap

	DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---	AC0
DDR4_A1	---	DDR3_A2	---	AC1
DDR4_A2	LPDDR4_A1_A	DDR3_A4	---	AC2
DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---	AC3
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	---	AC4
DDR4_A5	LPDDR4_A5_B	DDR3_A11	---	AC5
DDR4_A6	LPDDR4_A1_B	DDR3_A13	---	AC6
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	---	AC8
DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---	AC9
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10
DDR4_A11	LPDDR4_A0_A	DDR3_A7	---	AC11
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12
DDR4_A13	LPDDR4_A0_B	DDR3_A14	---	AC13
DDR4_A14	LPDDR4_A4_A	DDR3_A15	---	AC14
DDR4_A15	CASH	DDR3_A3	---	AC15
DDR4_A16	RASn	DDR3_RASn	---	AC16
DDR4_A17	CASn	DDR3_CASn	---	AC17
DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18
DDR4_BA1	LPDDR4_A4_B	DDR3_A12	---	AC19
DDR4_BA2	LPDDR4_ODT1_CA_B	DDR3_BA3	---	AC20
DDR4_BA3	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21
DDR4_CKE0	LPDDR4_CKE0_A	DDR3_CKE0	---	AC22
DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	---	AC23
DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	---	AC24
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	---	AC25
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_ODT1	---	AC26
DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	---	AC27
DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	---	AC28
DDR4_RESETh	LPDDR4_RESETh	DDR3_RESETh	---	AC29

Note: Sequences can not be swap



Caps should be placed under  
the U1000 package

RK3566  
BGA565\_15R50x14R40x0R90

**HAOYU ELECTRONICS** HAOYU Electronics Co., Ltd

Project: MarsBoard\_CM4\_SODIMM

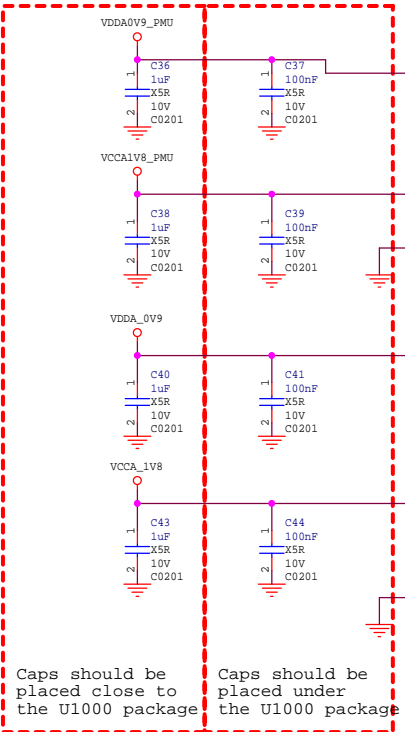
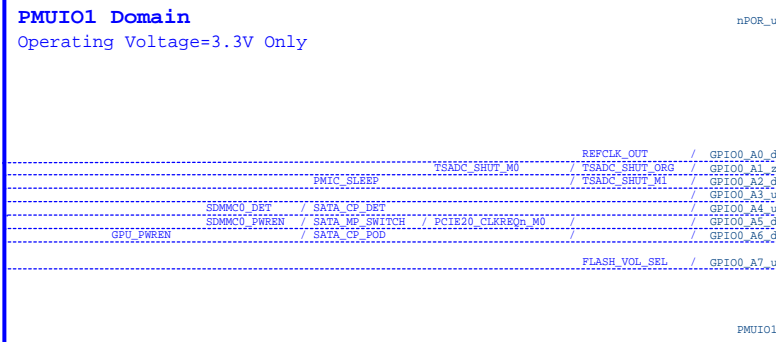
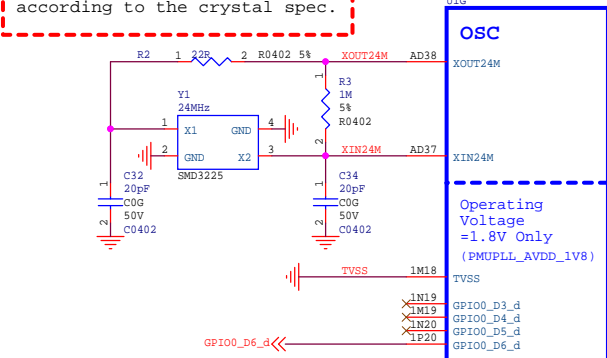
File: 03.RK3566\_DDR\_PHY

Date: Friday, November 04, 2022 Rev: V1.0

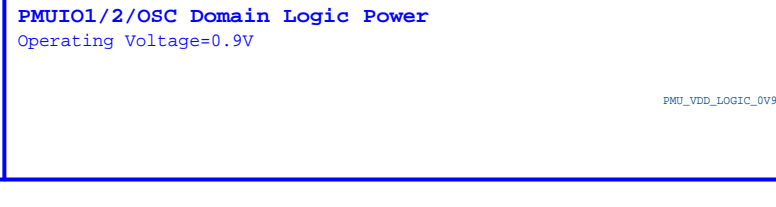
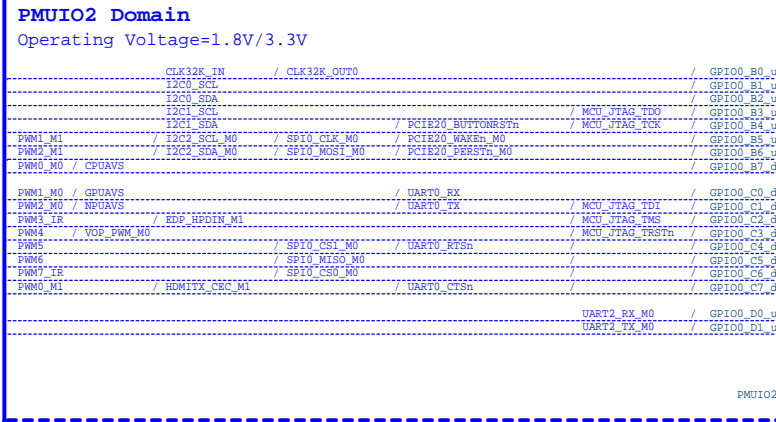
Designed by: Thomas Reviewed by: Thomas Sheet: 4 of 20

# RK3566\_G(OSC/PLL/PMUIO1/2)

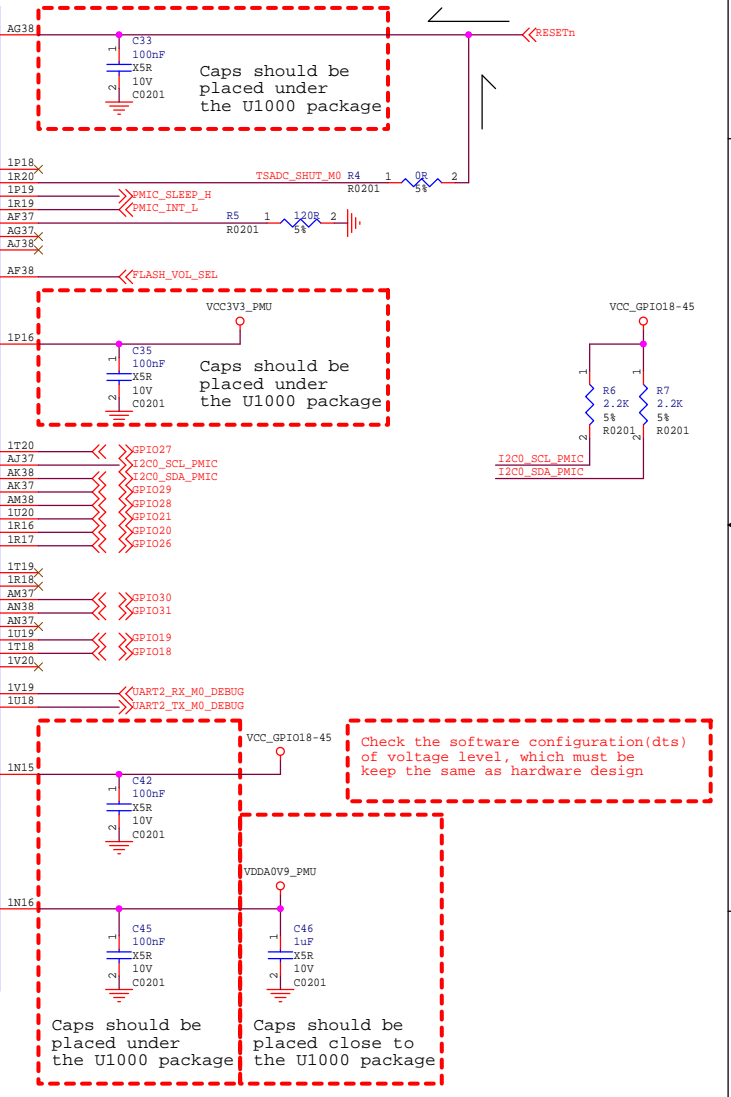
Adjust the load capacitor according to the crystal spec.



Caps should be placed close to the U1000 package. Caps should be placed under the U1000 package.



Caps should be placed under the U1000 package. Caps should be placed close to the U1000 package.



Caps should be placed under the U1000 package

Caps should be placed under the U1000 package

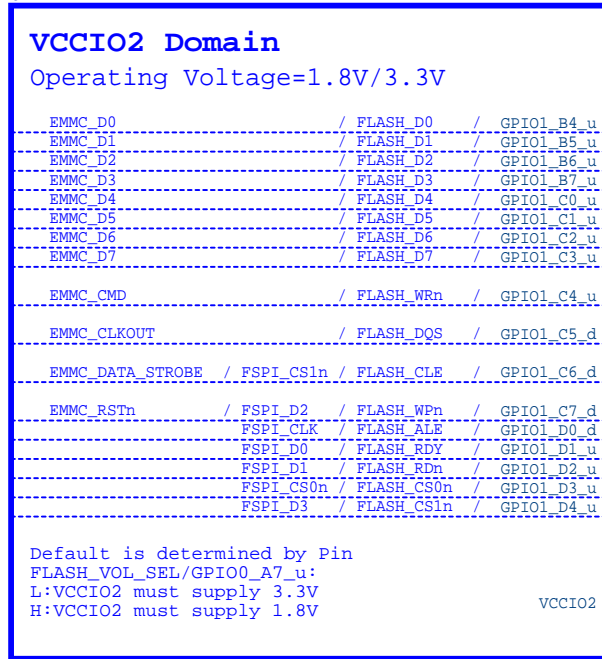
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

Caps should be placed under the U1000 package

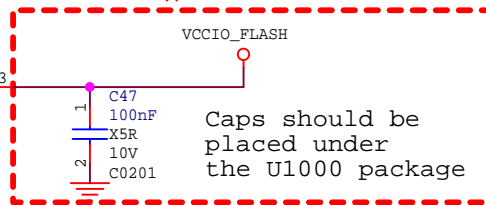
Caps should be placed close to the U1000 package

# RK3566\_I (VCCIO2 Domain)

U1I



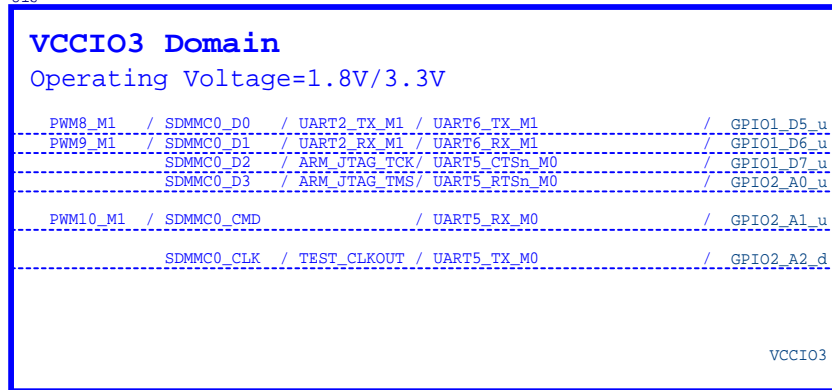
RK3566  
BGA565\_15R50x14R40x0R90



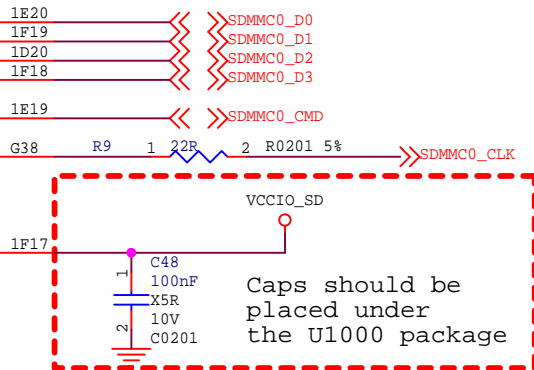
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

# RK3566\_J (VCCIO3 Domain)

U1J



RK3566  
BGA565\_15R50x14R40x0R90

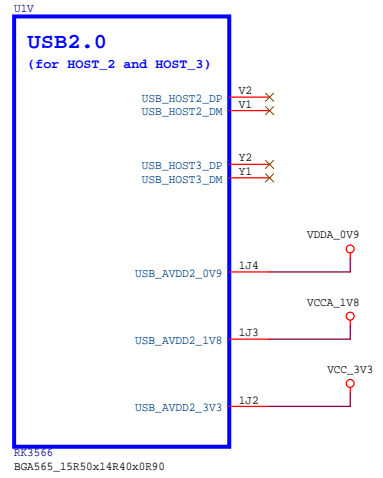
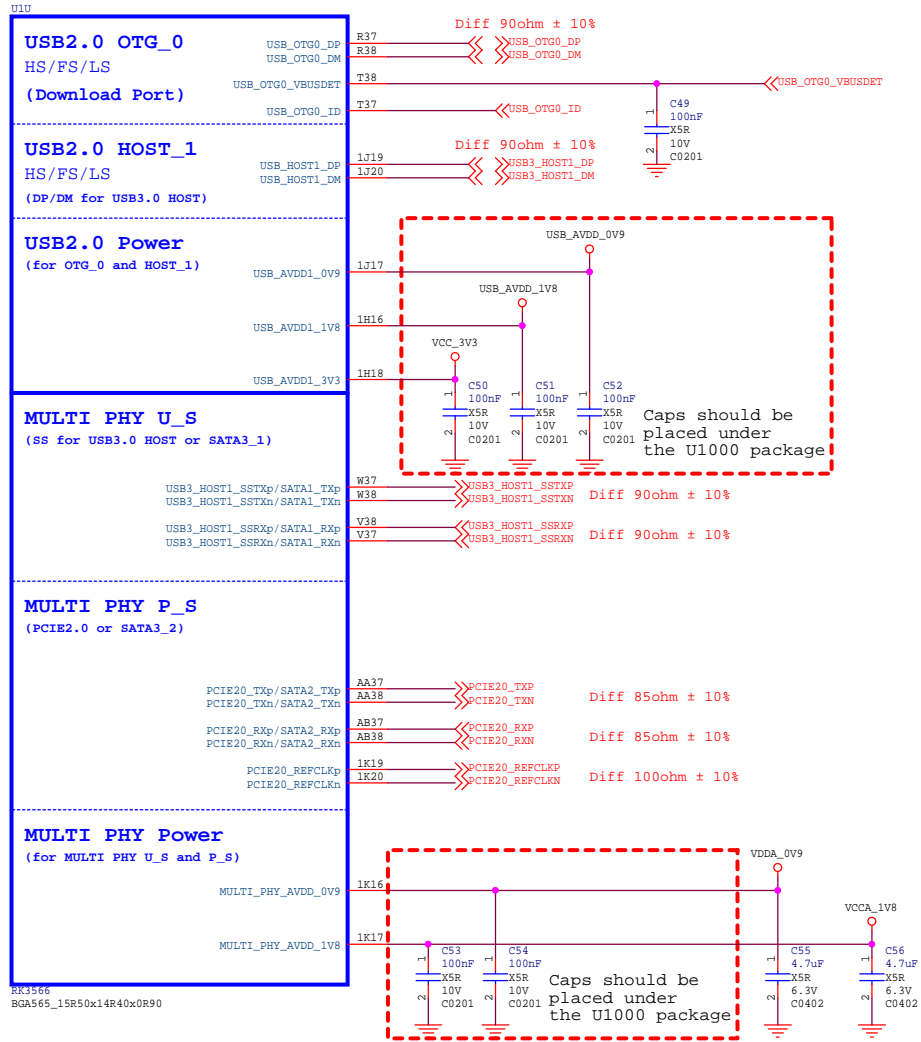


Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

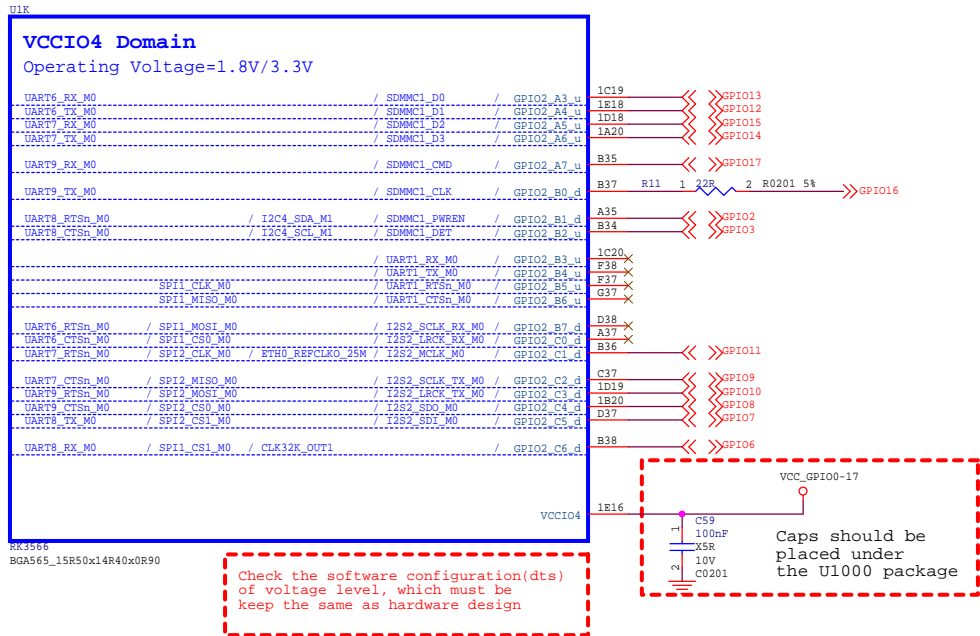
HAOYU Electronics Co., Ltd			
Project:	MarsBoard_CM4_SODIMM		
File:	05.RK3566_Flash/SD_Controller		
Date:	Friday, November 04, 2022	Rev:	V1.0
Designed by:	Thomas	Reviewed by:	Thomas
Sheet:	6 of 20		

# RK3566\_U(USB3.0/PCIe2.0x1/SATA)

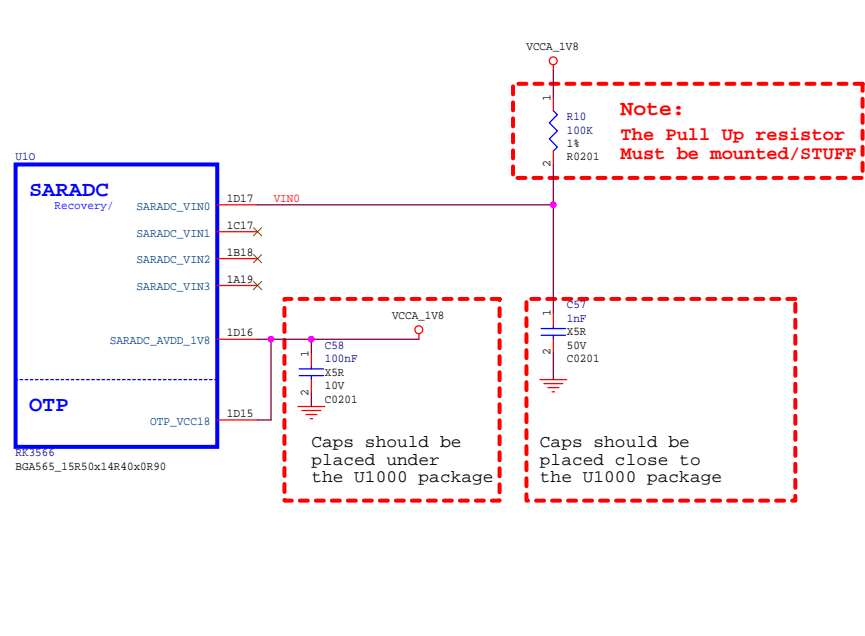
# RK3566\_V(USB2.0 HOST)



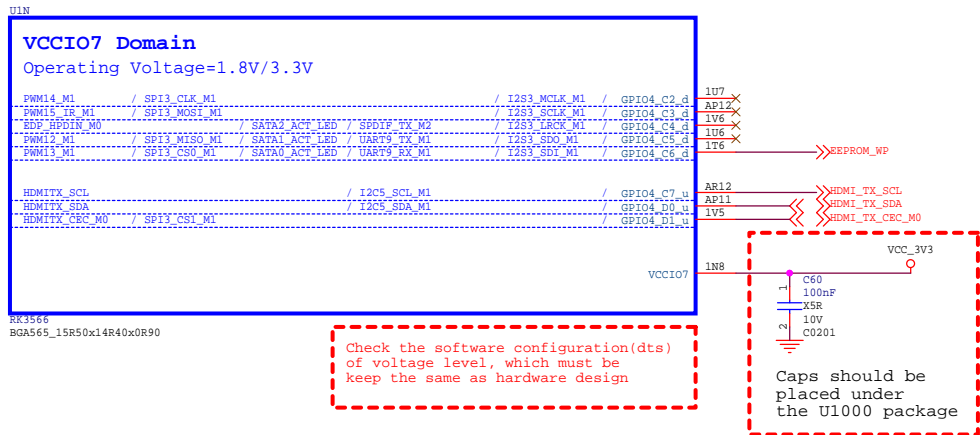
# RK3566\_K(VCCIO4 Domain)



# RK3566\_O(SARADC/OTP)



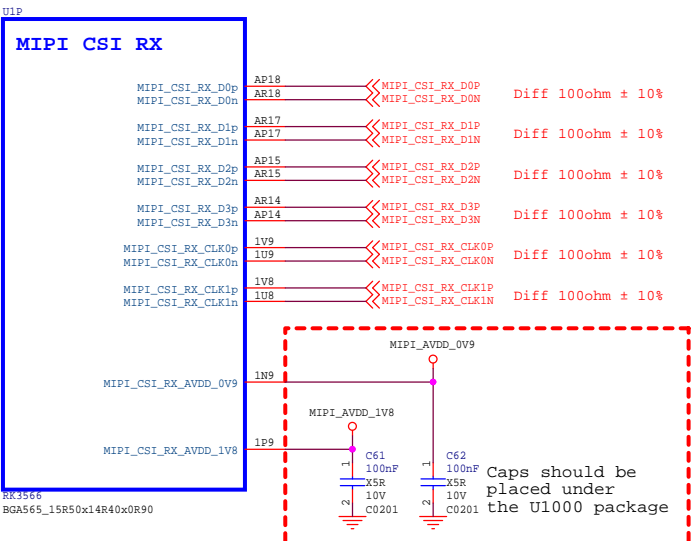
# RK3566\_N(VCCIO7 Domain)





# RK3566\_P(MIPI\_CSI\_RX)

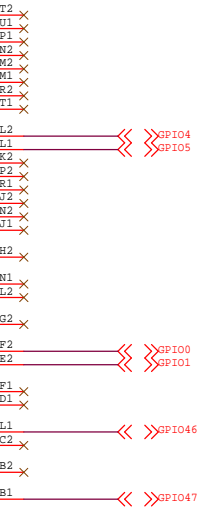
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1



# RK3566\_M(VCCIO6 Domain)

VCCIO6 Domain  
Operating Voltage=1.8V/3.3V

CIF_D0	/ EBC_SDD00 / SDMMC2_D0_M0 / I2S1_MCLK_M1 / VOP_BT656_D0_M1 / GPIO3_C6_d	IT2
CIF_D1	/ EBC_SDD01 / SDMMC2_D1_M0 / I2S1_SCLK_TX_M1 / VOP_BT656_D1_M1 / GPIO3_C7_d	IT1
CIF_D2	/ EBC_SDD02 / SDMMC2_D2_M0 / I2S1_LRCK_TX_M1 / VOP_BT656_D2_M1 / GPIO3_D0_d	AP1
CIF_D3	/ EBC_SDD03 / SDMMC2_D3_M0 / I2S1_SDO0_M1 / VOP_BT656_D3_M1 / GPIO3_D1_d	AN2
CIF_D4	/ EBC_SDD04 / SDMMC2_D4_M0 / I2S1_SDI0_M1 / VOP_BT656_D4_M1 / GPIO3_D2_d	AM2
CIF_D5	/ EBC_SDD05 / SDMMC2_D5_M0 / I2S1_SDI1_M1 / VOP_BT656_D5_M1 / GPIO3_D3_d	AM1
CIF_D6	/ EBC_SDD06 / SDMMC2_D6_M0 / I2S1_SDI2_M1 / VOP_BT656_D6_M1 / GPIO3_D4_d	IT2
CIF_D7	/ EBC_SDD07 / SDMMC2_D7_M0 / I2S1_SDI3_M1 / VOP_BT656_D7_M1 / GPIO3_D5_d	IT1
CIF_D8	/ EBC_SDD08 / GMAC1_TXD2_M1 / UART1_TX_M1 / PWM_CLK0_M1 / GPIO3_D6_d	AL2
CIF_D9	/ EBC_SDD09 / GMAC1_TXD3_M1 / UART1_RX_M1 / PWM_SD10_M1 / GPIO3_D7_d	AL1
CIF_D10	/ EBC_SDD010 / GMAC1_TXCLK_M1 / UART1_RX_M1 / PWM_CLK1_M1 / GPIO4_A0_d	AK2
CIF_D11	/ EBC_SDD011 / GMAC1_RXD2_M1 / UART1_TX_M2 / PWM_SD11_M1 / GPIO4_A1_d	IP2
CIF_D12	/ EBC_SDD012 / GMAC1_RXD3_M1 / UART1_TX_M2 / PWM_SD12_M1 / GPIO4_A2_d	IR1
CIF_D13	/ EBC_SDD013 / GMAC1_RXCLK_M1 / UART1_RX_M2 / PWM_SD13_M1 / GPIO4_A3_d	AT2
CIF_D14	/ EBC_SDD014 / GMAC1_RXD0_M1 / UART1_RX_M2 / I2S2_LRCK_TX_M1 / GPIO4_A4_d	IN2
CIF_D15	/ EBC_SDD015 / GMAC1_RXD1_M1 / UART1_RX_M2 / I2S2_LRCK_RX_M1 / GPIO4_A5_d	AJ1
ISP_FLASHTRIGOUT	/ EBC_SDCE0 / GMAC1_TXEN_M1 / SPI3_CS0_M0 / I2S1_SCLK_RX_M1 / GPIO4_A6_d	AH2
CAM_CLKOUT0	/ EBC_SDCE1 / GMAC1_RXD0_M1 / SPI3_CS1_M0 / I2S1_LRCK_RX_M1 / GPIO4_A7_d	IN1
CAM_CLKOUT1	/ EBC_SDCE2 / GMAC1_RXD1_M1 / SPI3_MISO_M0 / I2S1_SDO1_M1 / GPIO4_B0_d	IL2
ISP_PRELIGHT_TRIG	/ EBC_SDCE3 / GMAC1_RXDV_CRS_M1 / I2S1_SDO2_M1 / GPIO4_B1_d	AG2
I2C4_SDA_M0	/ EBC_VCOM / GMAC1_RXER_M1 / SPI3_MOSI_M0 / I2S2_SDI_M1 / GPIO4_B2_d	AF2
I2C4_SCL_M0	/ EBC_GDOE / PTH1_REPCLK0_25M_M1 / SPI3_CLK_M0 / I2S2_SDO_M1 / GPIO4_B3_d	AB2
ISP_FLASH_TRIGIN	/ I2C2_SDA_M1 / EBC_GDSP / GMAC1_RXD0_M1 / VOP_BT656_CLK_M1 / GPIO4_B4_d	AF1
I2C2_SCL_M1	/ EBC_SDSH / GMAC1_RXD1_M1 / I2S1_SDO3_M1 / GPIO4_B5_d	AD1
CIF_HREF	/ EBC_SDLB / GMAC1_MDC_M1 / UART1_RTSh_M1 / I2S2_MCLK_M1 / GPIO4_B6_d	IL1
CIF_VSYNC	/ EBC_SDOE / GMAC1_MDTG_M1 / UART1_RTSh_M1 / I2S2_SCLK_TX_M1 / GPIO4_B7_d	AC2
PWM1_IR_M1	/ CIF_CLKOUT / EBC_GDCLK / GMAC1_RXD0_M1 / I2S2_LRCK_TX_M1 / GPIO4_C0_d	AB2
CIF_CLKIN	/ EBC_SDCLK / GMAC1_MCLKINOUT_M1 / UART1_CTSh_M1 / I2S2_SCLK_RX_M1 / GPIO4_C1_d	AB1



**Note:**  
default VCCIO of Camera is 1.8V



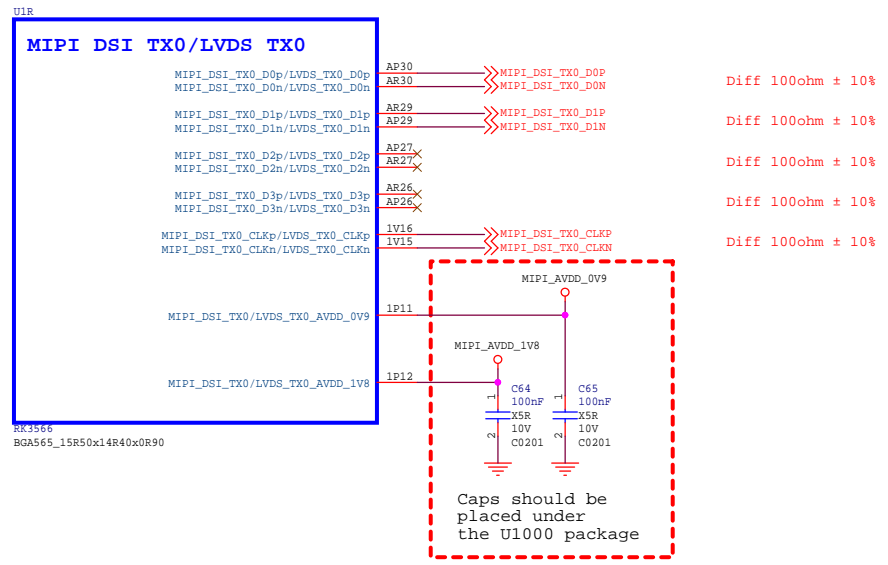
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

Caps should be placed under the U1000 package

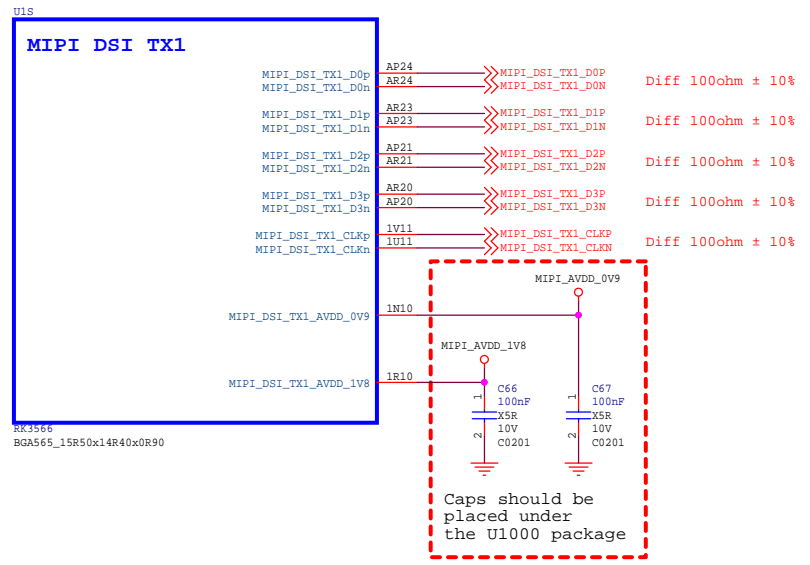
**HAOYU ELECTRONICS** HAOYU Electronics Co., Ltd

Project: MarsBoard\_CM4\_SODIMM  
 File: 08.RK3566\_VI\_Interface  
 Date: Friday, November 04, 2022  
 Designed by: Thomas Reviewed by: Thomas Sheet: 9 of 20

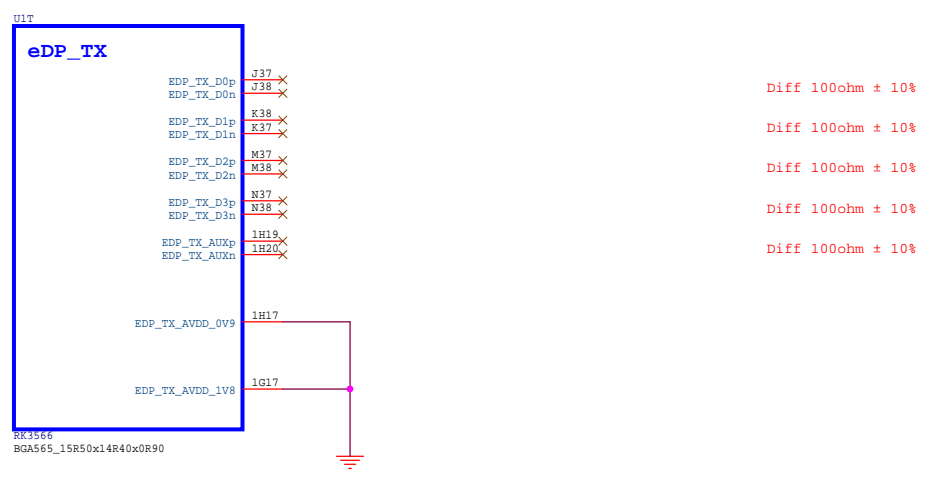
# RK3566\_R(MIPI\_DSI\_TX0/LVDS\_TX0)



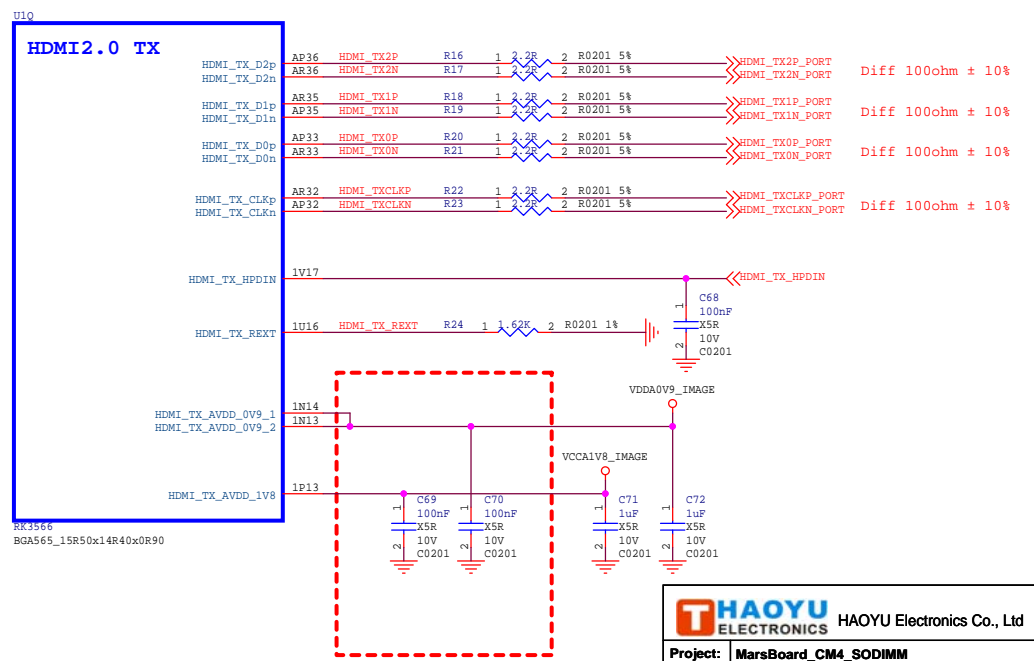
# RK3566\_S(MIPI\_DSI\_TX1)



# RK3566\_T(eDP TX)



# RK3566\_Q(HDMI2.0 TX)



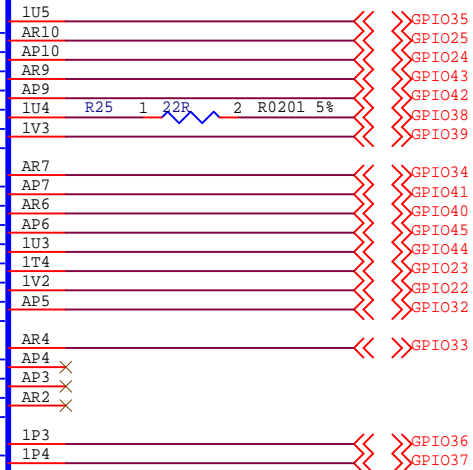
# RK3566\_L(VCCIO5 Domain)

U1L

## VCCIO5 Domain

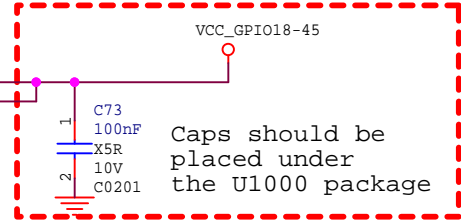
Operating Voltage=1.8V/3.3V

VOP_BT1120_D0	/ SPI1_CS0_M1			/ SDMMC2_D0_M1	/ GPIO3_A1_d
VOP_BT1120_D1		/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
VOP_BT1120_D2		/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
VOP_BT1120_D3		/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
VOP_BT1120_D4		/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
VOP_BT1120_CLK		/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
VOP_BT1120_D5		/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
VOP_BT1120_D6		/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1		/ GPIO3_B2_d
VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0		/ PDM_SDI0_M2	/ GPIO3_B3_d
VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0		/ PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0		/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0		/ GPIO3_B6_d
PWM12_M0		/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0		/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
VOP_BT1120_D13	/ SPI1_MOSI_M1		/ PCIE20_PERStn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
VOP_BT1120_D14	/ SPI1_MISO_M1		/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
VOP_BT1120_D15	/ SPI1_CLK_M1		/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d



RK3566  
BGA565\_15R50x14R40x0R90

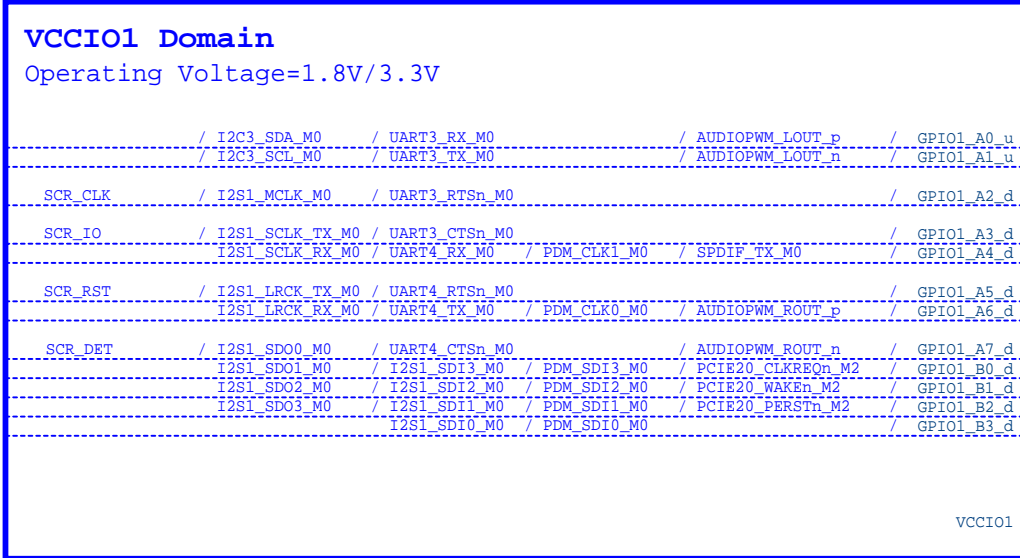
Check the software configuration(dts) of voltage level, which must be keep the same as hardware design



HAOYU Electronics Co., Ltd			
Project:	MarsBoard_CM4_SODIMM		
File:	10.RK3566_VO_Interface_2		
Date:	Friday, November 04, 2022	Rev:	V1.0
Designed by:	Thomas	Reviewed by:	Thomas
Sheet:	11	of	20

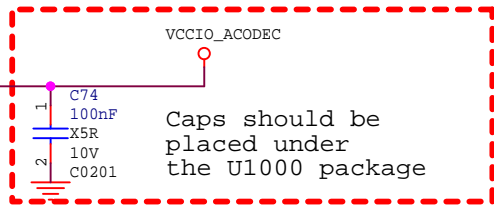
# RK3566\_H(VCCIO1 Domain)

U1H



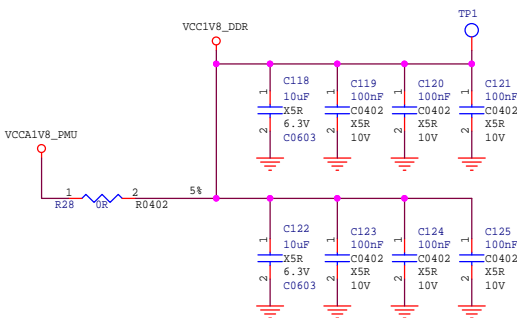
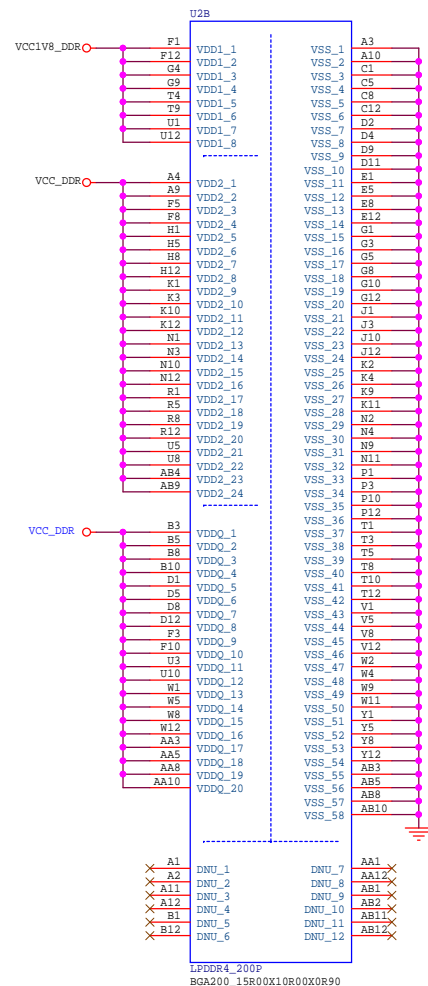
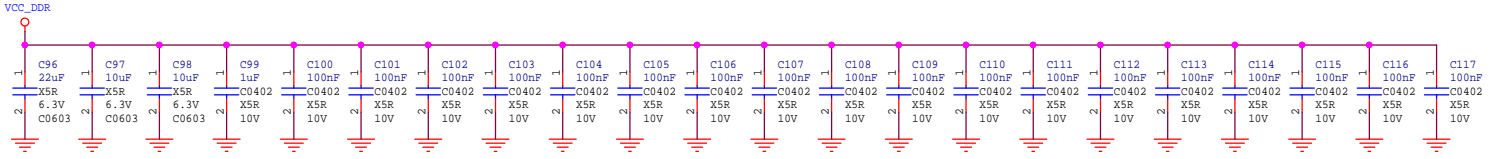
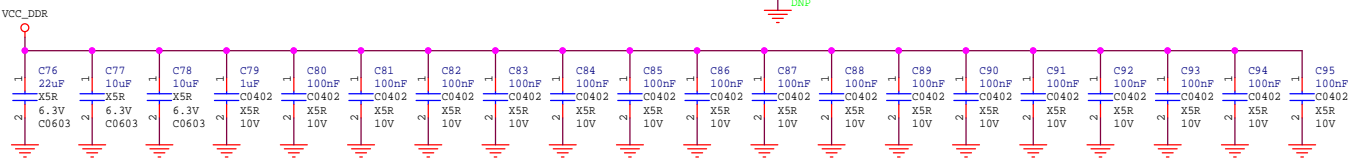
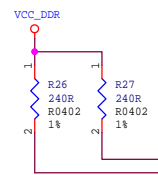
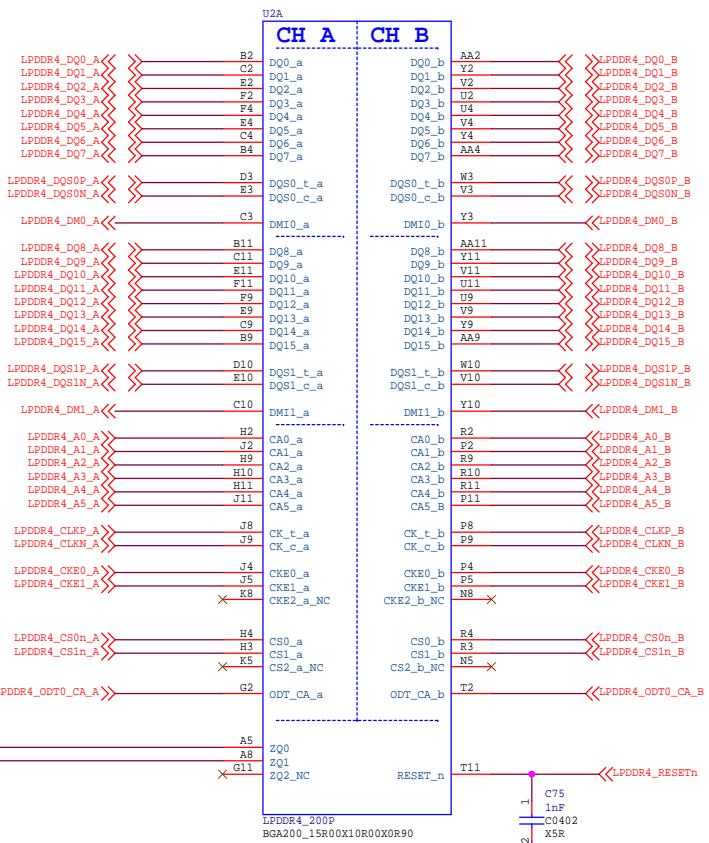
RK3566  
BGA565\_15R50x14R40x0R90

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

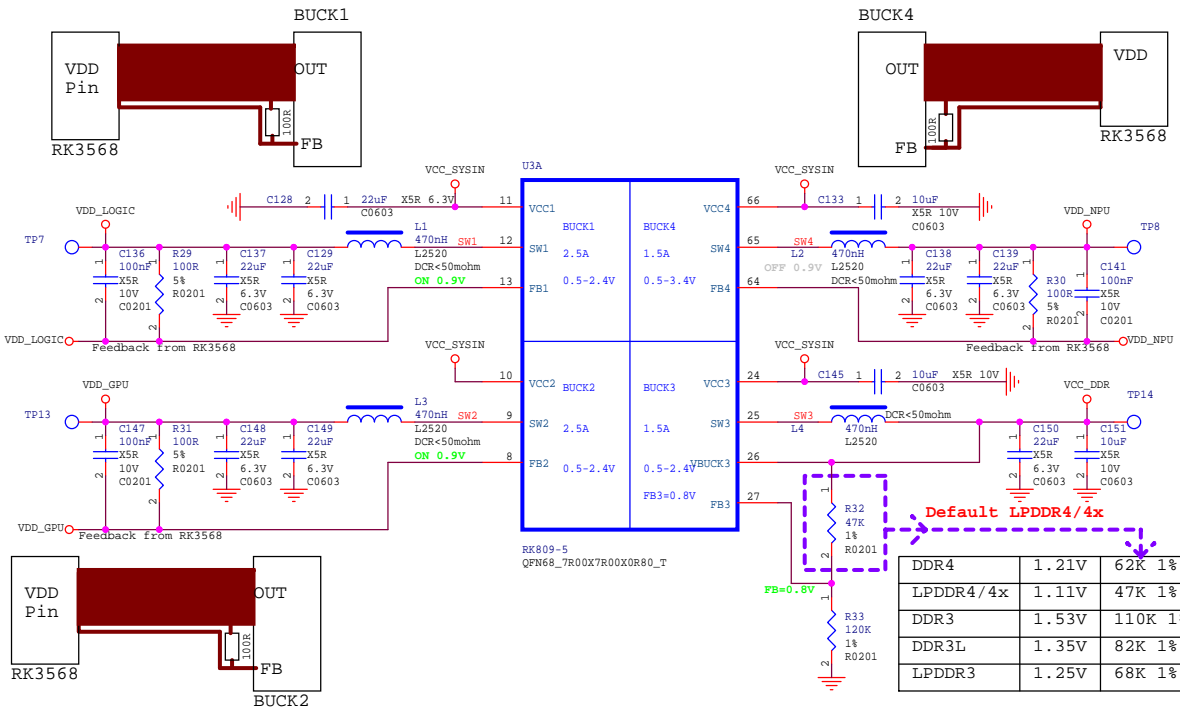


VCCIO1\_ACODEC = 3.3V as default

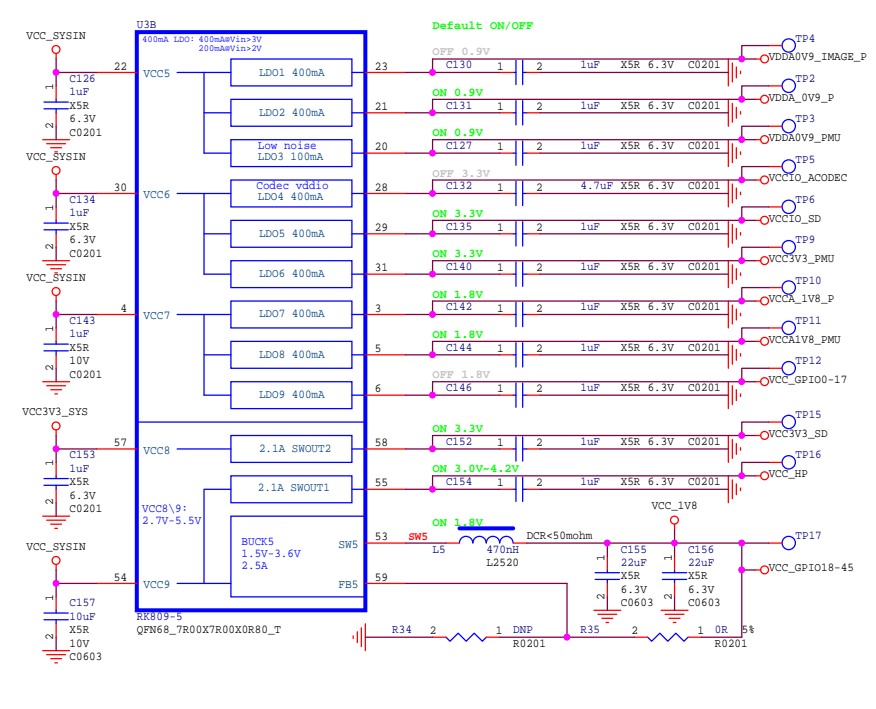
HAOYU Electronics Co., Ltd			
<b>Project:</b>	MarsBoard_CM4_SODIMM		
<b>File:</b>	11.RK3566_Audio_Interface		
<b>Date:</b>	Friday, November 04, 2022	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Thomas	<b>Reviewed by:</b>	Thomas
		<b>Sheet:</b>	12 of 20



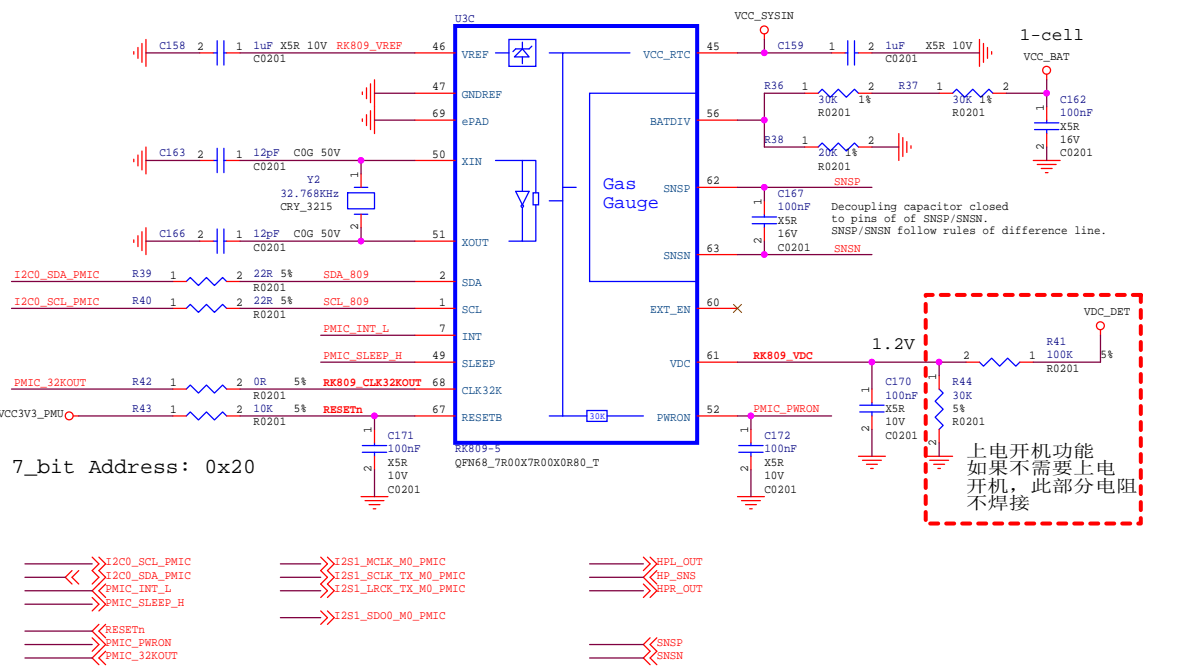
# PMIC RK809 DCDC



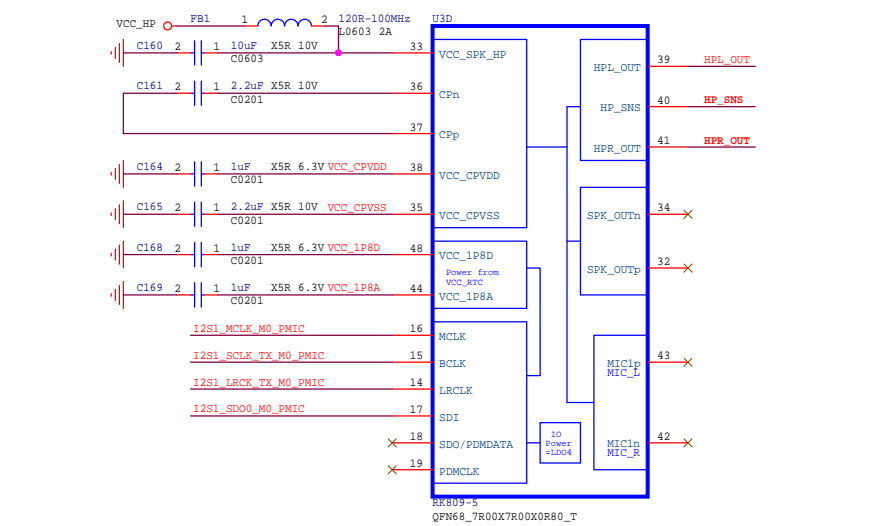
# PMIC RK809 LDO



# PMIC RK809 Management



# PMIC RK809 CODEC



**Note:**  
If RK809-5 codec is not used, then Pin 14,15,16,17,19,40 Tie VSS Pin 18,36,37,38,35,39,41,34,32,43,42 Leave floating

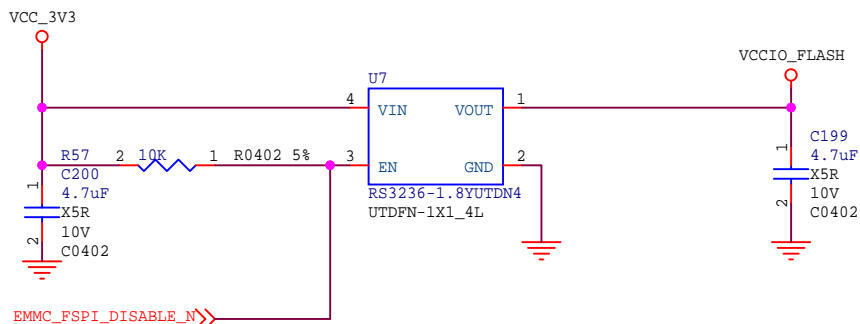
**HAOYU ELECTRONICS** HAOYU Electronics Co., Ltd

Project: MarsBoard\_CM4\_SODIMM  
 File: 13.Power\_Part3\_PMIC  
 Date: Friday, November 04, 2022  
 Designed by: Thomas



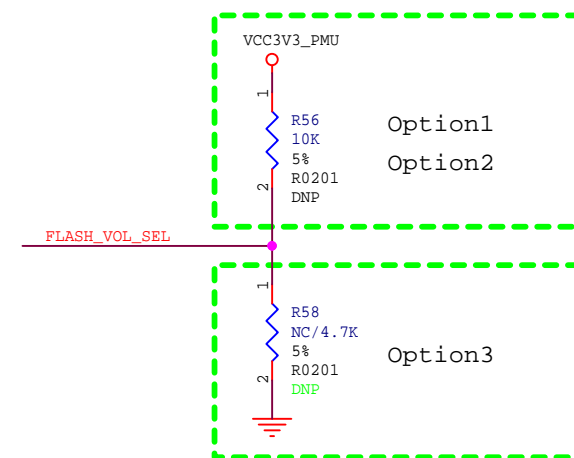
# Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



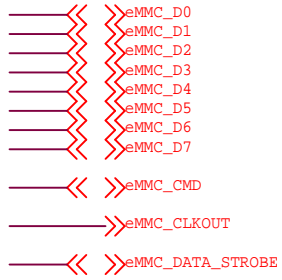
1. eMMC:  
Short 'EMMC\_FSPI\_DISABLE\_N' and GND to enter Maskrom Mode.
2. SPI Flash:  
Short 'EMMC\_FSPI\_DISABLE\_N' and GND to enter Maskrom Mode.

←←FLASH\_VOL\_SEL

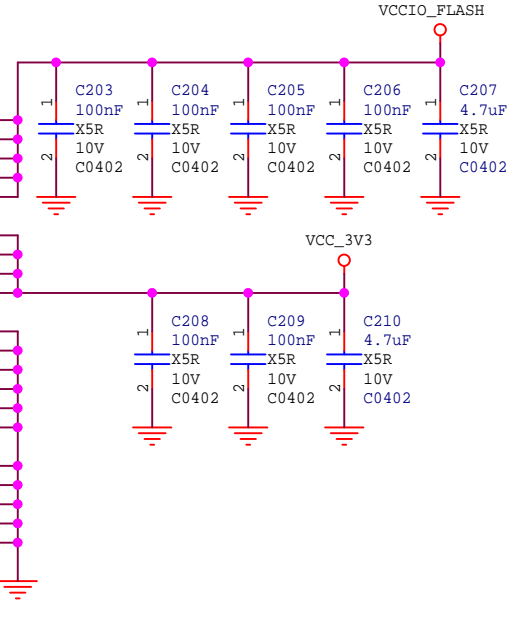
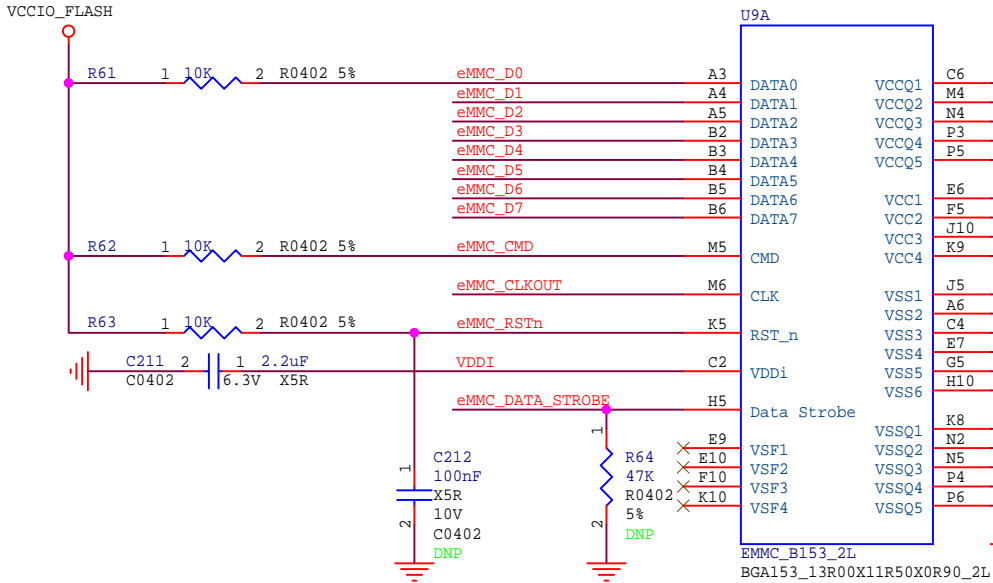


FLASH\_VOL\_SEL state decided to VCCIO2 domain IO driven by default  
Logic=L: 3.3V IO driven  
Logic=H: 1.8V IO driven

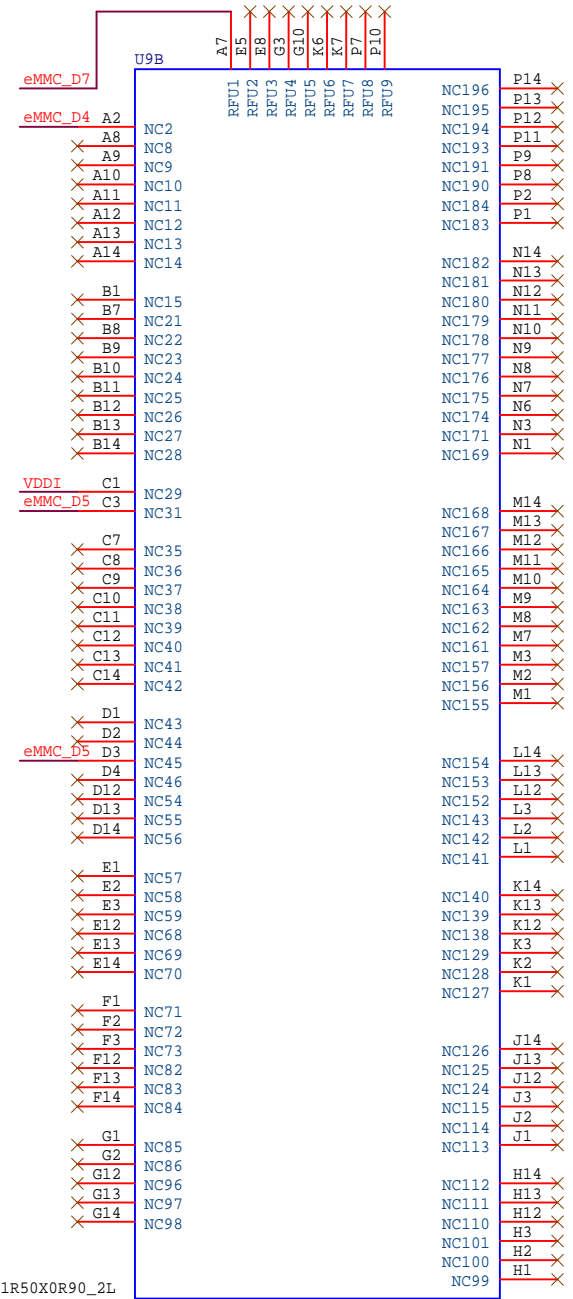




VCCIO\_FLASH



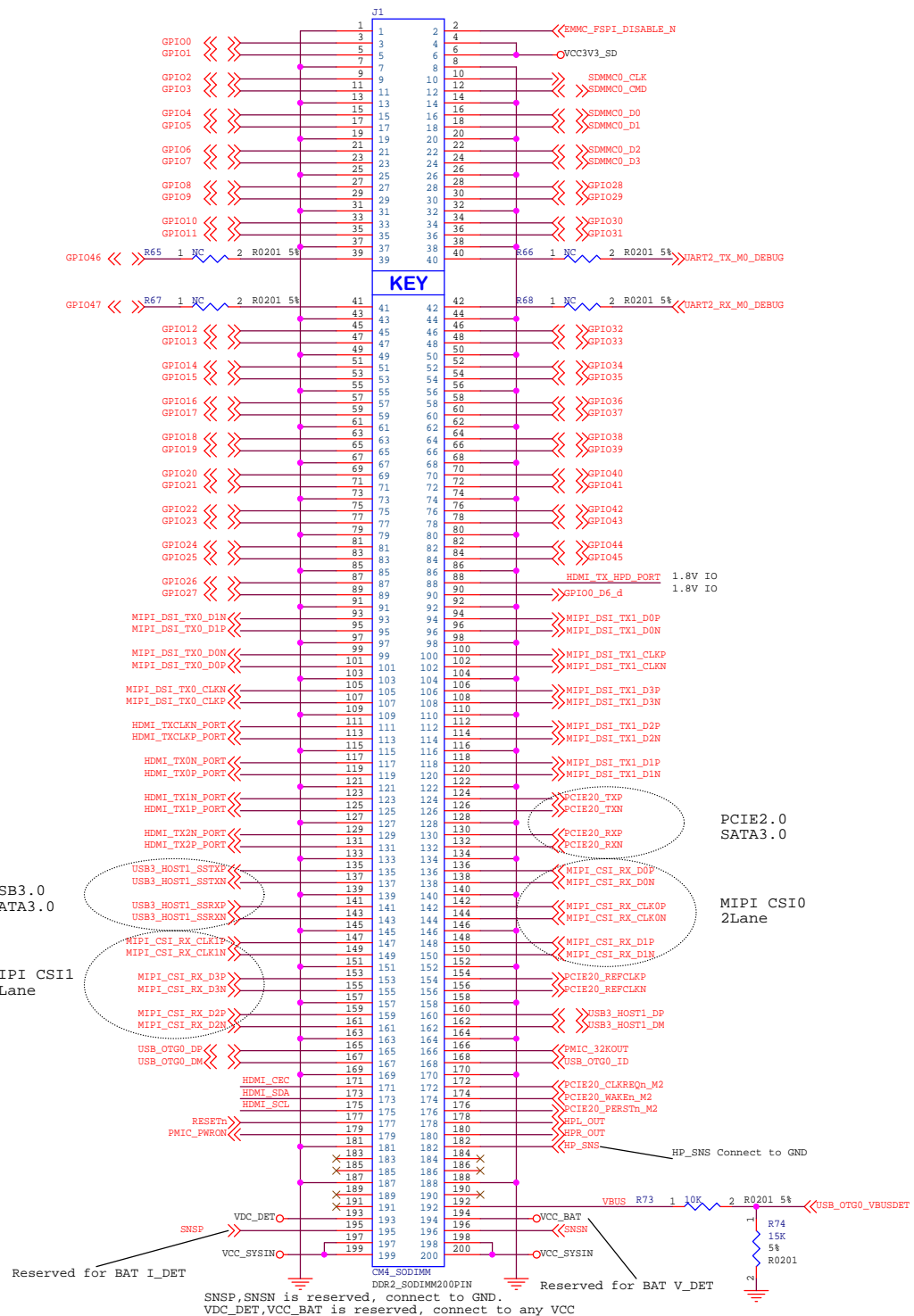
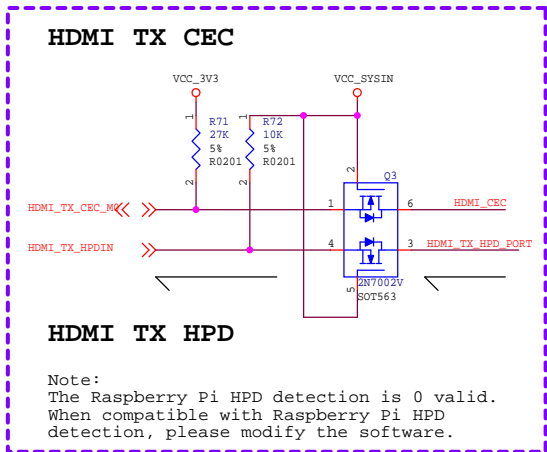
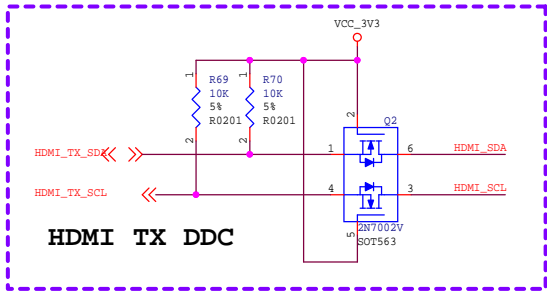
EMMC\_B153\_2L  
BGA153\_13R00X11R50X0R90\_2L



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<b>Project:</b>	MarsBoard_CM4_SODIMM		
<b>File:</b>	17.Flash-eMMC_Flash		
<b>Date:</b>	Friday, November 04, 2022	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Thomas	<b>Reviewed by:</b>	Thomas
		<b>Sheet:</b>	18 of 20

# CM4 SODIMM PINOUT

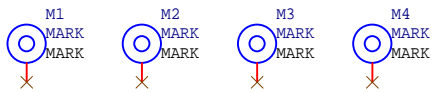


**HAOYU ELECTRONICS** HAOYU Electronics Co., Ltd

Project:	MarsBoard_CM4_SODIMM	Rev:	V1.0
File:	18.SODIMM_Pinout	Sheet:	19 of 20
Date:	Friday, November 04, 2022	Reviewed by:	Thomas
Designed by:	Thomas	Reviewed by:	Thomas


# Page of Accessories

## PCB Mark Point



## Mechanical Hole



 HAOYU Electronics Co., Ltd			
<b>Project:</b>	MarsBoard_CM4_SODIMM		
<b>File:</b>	19.Mark/Hole/Heatsink		
<b>Date:</b>	Friday, November 04, 2022	<b>Rev:</b>	V1.0
<b>Designed by:</b>	Thomas	<b>Reviewed by:</b>	Thomas
		<b>Sheet:</b>	20 of 20