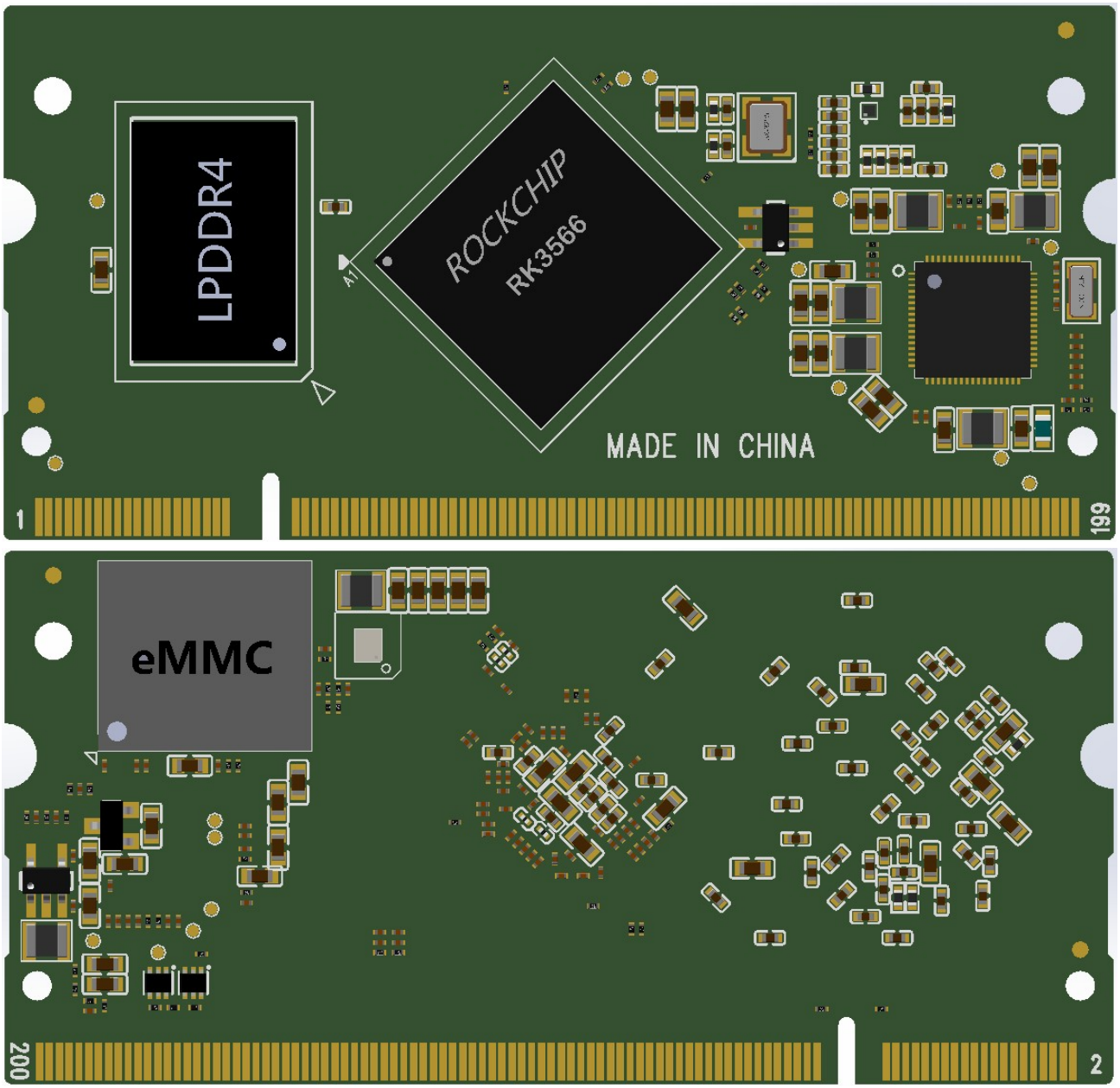
Chapter 1. Introduction

1.1. Introduction

Figure 1.
The RK3566 Compute Module 4 SODIMM (CM4S).



The RK3566 Compute Module 4 SODIMM (CM4S) is a System on Module (SoM) containing processor, memory, eMMC Flash, and supporting power circuitry. These modules allow a designer to leverage the RK3566 hardware and software stack in their own custom systems and form factors. In addition, these modules have extra GPIO over and above what is available on the RK3566 boards, opening up more options for the designer.

The design of the CM4S is compatible with Raspberry Pi Compute Module 4 SODIMM, and for cost-sensitive applications it can be supplied without the eMMC fitted; this version is called the RK3566 Compute Module 4 SODIMM Lite (RK3566 CM4SLite).

The CM4S is in the same form factor as the older Raspberry Pi Compute 3 and 3+ modules, which are mechanically compatible with DDR2-SODIMM.

NOTE

The CM4S SoC has a slightly increased z-height over the Raspberry Pi Compute Module 3.

NOTE

Unless otherwise stated, for this document CM4S also refers to CM4SLite.

1.2. Features

Key features of the CM4S are as follows:

- Rockchip RK3566, quad core Cortex-A55 (ARM v8) 64-bit SoC @ 1.8GHz with Arm Mali-G52 EE GPU, 0.8 TOPS NPU
- DDR2-SODIMM-mechanically-compatible form factor
- H.265 (HEVC) (upto 4Kp60 decode), H.264 (upto 1080p60 decode, 1080p30 encode)
- OpenGL ES 1.1/2.0/3.2， OpenCL 2.0， Vulkan 1.1
- Options for 1GB **(default)**/2GB/4GB LPDDR4-3200 SDRAM with ECC (see Appendix B)
- Options for 0GB **(CM4SLite)**, 32GB, 64GB, or 128GB eMMC flash memory (see Appendix B)
    - Peak eMMC bandwidth 100MBps (four times faster than previous Compute Modules)

- 1 × USB 2.0 OTG port (high speed)
- 1 × USB 2.0 host port
- 1 x USB 3.0 port
- 1 x PCIE2.1 port
- 2 x SATA 3.0 port (Multiplexing with USB3.0 and PCIE2.1 ports)
- 46 × GPIO supporting either 1.8V or 3.3V signalling and peripheral options:
    - Up to 10 × UART
    - Up to 4 × I2C

- Up to 2 × SPI
- 1 × SDIO interface
- 1 × PCM
- Up to 9× PWM channels

- 1 × HDMI 2.0 ports (up to 4Kp60 supported)
- MIPI DSI:
  - 1 × 2-lane MIPI DSI display port
  - 1 × 4-lane MIPI DSI display port
- MIPI CSI-2:
  - 2 × 2-lane MIPI CSI camera port
- 1 × SDIO 2.0 **(CM4SLite)**

IMPORTANT

The RK3566 Compute Module 4 SODIMM (CM4S) is intended for specific industrial customers migrating from Compute Module 4 SODIMM,Compute Module 3 or Compute Module 3+ and used as a substitute for these products.

Chapter 2. Interfaces

2.1. USB 2.0 OTG (high speed)

The USB 2.0 interface supports up to 480Mbps signalling. The differential pair should be routed as a 90Ω differential pair. The length of the P/N signals should ideally be matched to better than 0.15mm.

NOTE

The port is capable of being used as a true USB On-The-Go (OTG) port. While there is no official documentation, some users have had success making this work. The USB_OTGID pin is used to select between USB host and device that is typically wired to the ID pin of a Micro USB connector. To use this functionality it must be enabled in the OS. If using either as a fixed slave or fixed master, please tie the USB_OTGID pin to ground.

2.2. GPIO

There are 46 pins available for general purpose I/O (GPIO); 28 of them correspond to the GPIO pins on the Raspberry Pi 4 Model B 40-pin header. The 46 pins have access to internal peripherals:GMAC, I2C, PWM, SPI, and UART. The Rockchip RK3566 TRM describes these features in detail, along with the multiplexing options available. The drive strength and slew rate should ideally be set as low as possible to reduce any EMC issues.

The RK3566 GPIO bank0 is powered by GPIO0-17_VDD, and GPIO bank1 is powered by GPIO18-47_VDD. These can either be connected to +1.8V for 1.8V signalling GPIO, or +3.3V for 3.3V signalling. You should keep the load on each GPIO bank to below 50mA in total. GPIO0-17_VDD and GPIO18-47_VDD must be powered for the CM4S to start up correctly.

2.2.1. Alternative function assignments

Up to six alternative functions are available. The BCM2711 ARM peripherals book describes these features in detail. The table below gives a quick overview.

Table 1. GPIO pins alternative function assignment

GPIO	Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
GPIO0	Low	GPIO4_B2_d	I2C4_SDA_M0	EBC_VCOM	GMAC1_RXER_M1	SPI3_MOSI_M0	I2S2_SDI_M1
GPIO1	Low	GPIO4_B3_d	I2C4_SCL_M0	EBC_GDOE	ETH1_REFCLKO_25M_M1	SPI3_CLK_M0	I2S2_SDO_M1
GPIO2	Low	GPIO2_B1_d	SDMMC1_PWRE	I2C4__SDA_M1	UART8_RTSn_M0	CAN2_RX_M1	
GPIO3	High	GPIO2_B2_u	SDMMC1_DET	I2C4__SCL_M1	UART8_CTSn_M0	CAN2_TX_M1	

GPIO	Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
GPIO4	Low	GPIO3_D6_d	CIF_D8	EBC_SDDO8	GMAC1_TXD2_M1	UART1_TX_M1	PDM_CLK0_M1
GPIO5	Low	GPIO3_D7_d	CIF_D9	EBC_SDDO9	GMAC1_TXD3_M1	UART1_RX_M1	PDM_SDI0_M1
GPIO6	Low	GPIO2_C6_d	CLK32K_OUT1	UART8_RX_M0	SPI1_CS1_M0		
GPIO7	Low	GPIO2_C5_d	I2S2_SDI_M0	UART8_TX_M0	SPI2_CS1_M0		
GPIO8	Low	GPIO2_C4_d	I2S2_SDO_M0	UART9_CTSn_M0	SPI2_CS0_M0		

GPIO9	Low	GPIO2_C2_d	I2S2_SCLK_TX_M0	UART7_CTSn_M0	SPI2_MISO_M0		
GPIO10	Low	GPIO2_C3_d	I2S2_LRCK_TX_M0	UART9_RTSn_M0	SPI2_MOSI_M0		
GPIO11	Low	GPIO2_C1_d	I2S2_MCLK_M0	ETH0_REFCLKO_25M	UART7_RSTn_M0	SPI2_CLK_M0	
GPIO12	High	GPIO2_A4_u	SDMMC1_D1	UART6_TX_M0			
GPIO13	High	GPIO2_A3_u	SDMMC1_D0	UART6_RX_M0			
GPIO14	High	GPIO2_A6_u	SDMMC1_D3	UART7_TX_M0			
GPIO15	High	GPIO2_A5_u	SDMMC1_D2	UART7_RX_M0			
GPIO16	Low	GPIO2_B0_d	SDMMC1_CLK	UART9_TX_M0			
GPIO17	High	GPIO2_A7_u	SDMMC1_CMD	UART9_RX_M0			
GPIO18	Low	GPIO0_C6_d	PWM7_IR	SPI0_CS0_M0			
GPIO19	Low	GPIO0_C5_d	PWM6	SPI0_MISO_M0			
GPIO20	High	GPIO0_B6_u	I2C2_SDA_M0	SPI0_MOSI_M0	PCIE20_PERSTn_M0	PWM2_M1	
GPIO21	High	GPIO0_B5_u	I2C2_SCL_M0	SPI0_CLK_M0	PCIE20_WAKEn_M0	PWM1_M1	
GPIO22	Low	GPIO3_B6_d	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	
GPIO23	Low	GPIO3_B5_d	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	
GPIO24	Low	GPIO3_A3_d	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	
GPIO25	Low	GPIO3_A2_d	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	
GPIO26	Low	GPIO0_B7_d	PWM0_M0	CPU_AVS			
GPIO27	High	GPIO0_B0_u	CLK32K_IN	CLK32K_OUT0			
GPIO28	High	GPIO0_B4_u	I2C1_SDA	PCIE20_BUTTONRSTn	MCU_JTAG_TCK	CAN0_RX_M0	
GPIO29	High	GPIO0_B3_u	I2C1_SCL	MCU_JTAG_TDO		CAN0_TX_M0	
GPIO30	Low	GPIO0_C2_d	PWM3_IR	EDP_HPDIN_M1	MCU_JTAG_TMS		
GPIO31	Low	GPIO0_C3_d	PWM4	VOP_PWM_M0	MCU_JTAG_TRSTn		
GPIO32	Low	GPIO3_B7_d	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	
GPIO33	Low	GPIO3_C0_d	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	
GPIO34	Low	GPIO3_B0_d	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0	SDMMC2_PWR		
GPIO35	Low	GPIO3_A1_d	VOP_BR1120_D0	SPI1_CS0_M1	SDMMC2_D0_M1		

2.2. GPIO

GPIO	Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
GPIO36	Low	GPIO3_C4_d	PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2
GPIO37	Low	GPIO3_C5_d	PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2
GPIO38	Low	GPIO3_A6_d	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	
GPIO39	Low	GPIO3_A7_d	VOP_BT1120_D5	GMAC1_RXCLK_M0	SDMMC2_DET_M1		
GPIO40	Low	GPIO3_B2_d	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	
GPIO41	Low	GPIO3_B1_d	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	
GPIO42	Low	GPIO3_A5_d	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	
GPIO43	Low	GPIO3_A4_d	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	
GPIO44	Low	GPIO3_B4_d	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	
GPIO45	Low	GPIO3_B3_d	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	
GPIO46	Low	GPIO4_B6_d	CIF_HREF	EBC_SDLE	GMAC1_MDC_M1	UART1_RTSn_M1	
GPIO47	Low	GPIO4_C1_d	CIF_CLKIN	EBC_SDCLK	GMAC1_MCLKINOUT_M1	UART1_CTSn_M1	

2.3. HDMI 2.0

The CM4S supports one HDMI 2.0 interface capable of driving 4K images.

HDMI signals should be routed as 100Ω differential pairs. Each signal within a pair should ideally be matched to better than 0.15mm. Pairs don't typically need any extra matching, as they only have to be matched to 25mm.

CEC is also supported; an internal 27kΩ pullup resistor is included in the CM4S.

2.4. CSI-2 (MIPI serial camera)

The CM4S supports two camera ports: CAM0 (2 lanes) and CAM1 (2 lanes). CSI signals should be routed as 100Ω differential pairs. Each signal within a pair should ideally be matched to better than 0.15mm.

NOTE

The official RK3566 firmware supports the OmniVision OV5647, Sony IMX219 and Sony IMX477 camera sensors. No security device is required on Compute Module devices in order to use these camera sensors.

2.5. DSI (MIPI serial display)

The CM4S supports two display ports: DISP0 (2 lanes) and DISP1 (4 lanes). Each lane supports a maximum data rate per lane of 1Gbps.

Although Linux kernel drivers are available, the DSI interface is not currently documented. Only DSI displays supported by the official RK3566 firmware are supported. DSI signals should be routed as 100Ω differential pairs; each signal within a pair should ideally be matched to better than 0.15mm.

NOTE

The CM4S supports up to two displays of any type (HDMI, DSI,) at any one time.

2.6. SDIO/eMMC (CM4SLite only)

The CM4SLite does not have on-board eMMC. The eMMC signals are available on the connector so that an external eMMC or SD card can be used.

The SDX_VDD signal is used to power the CM4SLite SDIO/eMMC interface and can therefore be used to set the SDIO voltage to either +3.3V or +1.8V.

2.7. RUN (RESETn)

This pin when high signals that the CM4S has started. Driving this pin low resets the module. This should be done with caution; if files on a filesystem are open they will not be closed.

2.8. EMMC_DISABLE_N

When this pin is set to a low level signal, RK3566 does not boot from SD card or eMMC, and enters MARKROM mode at this time, forcing USB boot to enter download mode. Can be used to download eMMC firmware. This pin is internally pulled up to 3.3V via a 10kΩ resistor.

2.9. ACT_LED_1V8 (GPIO0_D6_d)

This pin is driven low to signal that connected to a LED

2.10. EEPROM_nWP (GPIO4_C6_d)

It is recommended to set this IO to low level to prevent end users changing the contents of the onboard EEPROM.

Chapter 3. Electrical and mechanical

3.1. Mechanical

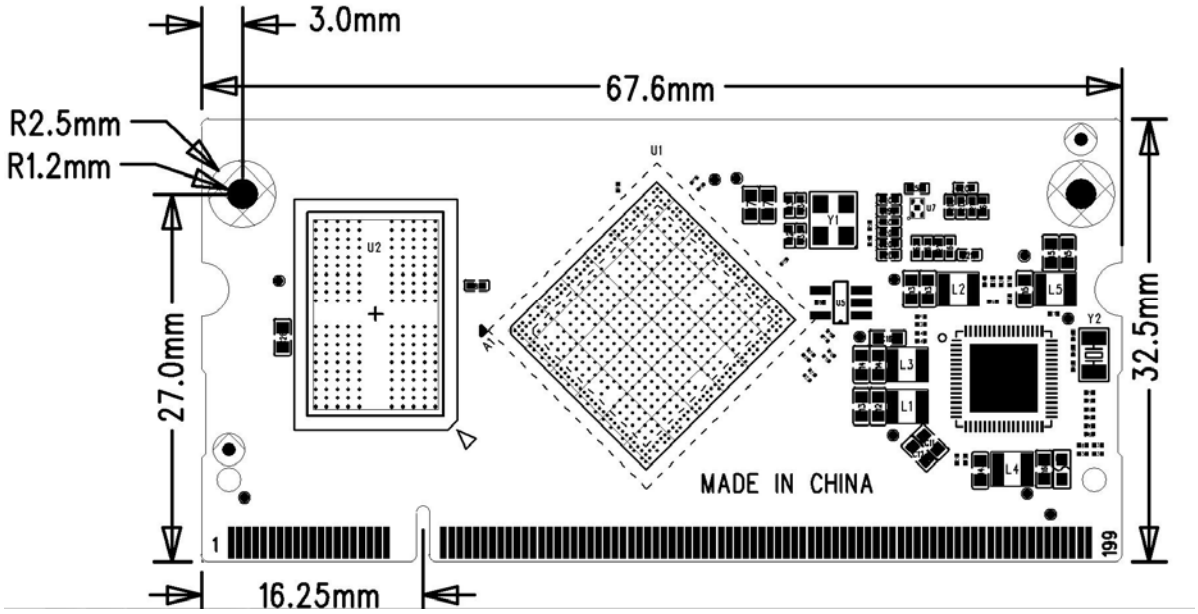
The CM4S modules conform to JEDEC MO-224 mechanical specification for 200-pin DDR2 (1.8V) SODIMM modules, so should work with the many DDR2 SODIMM sockets available on the market.

NOTE

The pinout of the CM4S is not the same as a DDR2 SODIMM module; they are **not** electrically compatible.

1. 2 × M2 mounting holes (inset 3mm from module edge).
2. PCB thickness 1mm ± 10%.
3. RK3566 SoC height including solder balls 0.794 ± 0.1mm.
4. The maximum component height on the underside of the Compute Module is 1.4mm.
5. The maximum component height on the top side of the Compute Module is 1.4mm.

Figure 2. Mechanical specification of the RK3566 Compute Module 4 SODIMM



NOTE

The location and arrangement of components on the Compute Module may change slightly over time due to revisions for cost and manufacturing considerations; however the maximum component heights and PCB thickness will be kept as specified.

A step file of the CM4S is available as part of the CM4S design data package. This is for guidance only and is subject to changes over time due to revisions.

3.2. Thermal

The RK3566 will reduce the clock rate to try and keep its internal temperature below 85°C. So in high ambient temperatures it is possible that the clock will also be automatically throttled back. If the RK3566 is unable to lower its

internal clocks enough to bring the temperature down, its case temperature will rise above 85°C. It is important that any thermal solution chosen keeps the ambient temperature for the other silicon devices on the CM4S within the operating temperature range.

Operating temperature range: -20°C - +85°C non-condensing.

3.3. Electrical specification

WARNING

Stresses above those listed in Table 3 may cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{BAT}	Core Power Supply	-0.5	5.5	V
V_{3V3}	+3.3V Supply	-0.5	3.6	V
$V_{GPIOx\text{-}y\_VDD}$	GPIO Voltage	-0.5	3.6	V
V_{SDX_VDD}	SDIO Voltage	-0.5	3.6	V
V_{gpio}	GPIO Input voltage	-0.5	$V_{GPIOx\text{-}y\_VDD}$ + 0.5	V

Table 4. Operating ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{BAT}	Core Power Supply	2.5	5.25	V
V_{3V3}	+3.3V Supply	3.15	3.45	V
$V_{GPIOx\text{-}y\_VDD}$	GPIO Voltage	1.71	3.45	V
V_{SDX_VDD}	SDIO Voltage	1.71	3.45	V

NOTE

$V_{GPIOx\text{-}y\_VDD}$ is the GPIO bank voltage (either GPIO0-17_VDD or GPIO18-45_VDD), each of which must be tied to either the 3.3V or the 1.8V rail of the CM4S.

Table 5. DC characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IL(gpio)}$	Input low voltage	$V_{GPIOx-y\_VDD}$ = 3.3V	0	-	0.8	V
$V_{IH(gpio)}$	Input high voltage	$V_{GPIOx-y\_VDD}$ = 3.3V	2.0	-	$V_{GPIOx-y\_VDD}$	V
$V_{IL(gpio)}$	Input low voltage	$V_{GPIOx-y\_VDD}$ = 1.8V	0	-	0.35	V
$V_{IH(gpio)}$	Input high voltage	$V_{GPIOx-y\_VDD}$ = 1.8V	0.65	-	$V_{GPIOx-y\_VDD}$	V

3.3. Electrical specification

$I_{IL(gpio)}$	Input leakage current	-	-	-	10	µA
$V_{OL(gpio)}$	Output low voltage	-	-	-	0.4	V
$V_{OH(gpio)}$	Output high voltage	-	$V_{GPIOx-y\_VDD}$ - 0.4	-	-	V
$I_{O(gpio)}$	Output current	1mA	0.87	1.3	-	mA
$I_{O(gpio)}$	Output current	2mA	1.75	2.6	-	mA
$I_{O(gpio)}$	Output current	3mA	2.63	3.9	-	mA
$I_{O(gpio)}$	Output current	4mA **default**	3.5	5.3	-	mA
$I_{O(gpio)}$	Output current	5mA	4.39	6.6	-	mA
$I_{O(gpio)}$	Output current	6mA	5.27	7.9	-	mA
$I_{O(gpio)}$	Output current	7mA	6.15	9.2	-	mA
$I_{O(gpio)}$	Output current	8mA	7.02	10.5	-	mA
$R_{PU(gpio)}$	Pullup resistor	$V_{GPIOx-y\_VDD}$ = 3.3V	33	47	73	kΩ
$R_{PD(gpio)}$	Pulldown resistor	$V_{GPIOx-y\_VDD}$ = 3.3V	33	47	73	kΩ
$R_{PU(gpio)}$	Pullup resistor	$V_{GPIOx-y\_VDD}$ = 1.8V	18	47	73	kΩ
$R_{PD(gpio)}$	Pulldown resistor	$V_{GPIOx-y\_VDD}$ = 1.8V	18	47	73	kΩ

Refer to interface specifications (see Chapter 2) for electrical details of other interfaces.

Table 6. Power consumption

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
P_{idle}	Idle power		-	1.5	-	W
P_{load}	Operational power		-	7	-	W
P_{VBAT}	Vbat power		-	7	-	W
$P_{3.3V}$	3.3V power		-	1	-	W

NOTE

The figures in Table 6 greatly depend on the end application.

Chapter 4. Pinout

Pin	Signal	Description
1	GND	Ground (0V)
2	EMMC_DISABLE_N	Drive low to force USB boot. (enter MARKROM mode) Internal 10kΩ pull up to 3.3V must be driven by an open collector signal.
3	GPIO0	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
4	SDX_VDD	SD card/eMMC IO supply: typically +3.3V, but can be 1.8V if external eMMC supports 1.8V signalling.
5	GPIO1	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
6	SDX_VDD	SD card/eMMC IO supply: typically +3.3V, but can be made 1.8V if external eMMC supports 1.8V signalling.
7	GND	Ground (0V)
8	GND	Ground (0V)
9	GPIO2	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
10	SDX_CLK	SD card/eMMC clock signal (only available on CM4SLite).
11	GPIO3	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
12	SDX_CMD	SD card/eMMC command signal (only available on CM4SLite).
13	GND	Ground (0V)
14	GND	Ground (0V)
15	GPIO4	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
16	SDX_D0	SD card/eMMC Data0 signal (only available on CM4SLite).
17	GPIO5	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
18	SDX_D1	SD card/eMMC Data1 signal (only available on CM4SLite).
19	GND	Ground (0V)
20	GND	Ground (0V)
21	GPIO6	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
22	SDX_D2	SD card/eMMC Data2 signal (only available on CM4SLite).
23	GPIO7	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.

Table 7. Pinout for the RK3566 Compute Module 4 SODIMM

24	SDX_D3	SD card/eMMC Data3 signal (only available on CM4SLite).
25	GND	Ground (0V)
26	GND	Ground (0V)

27	GPIO8	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
28	GPIO28	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
29	GPIO9	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
30	GPIO29	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
31	GND	Ground (0V)
32	GND	Ground (0V)
33	GPIO10	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
34	GPIO30	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
35	GPIO11	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
36	GPIO31	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
37	GND	Ground (0V)
38	GND	Ground (0V)
39	GPIO46	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
40	UART2_TX_DEBUG	RK3566 debugging port
41	GPIO47	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
42	UART2_RX_DEBUG	RK3566 debugging port
43	GND	Ground (0V)
44	GND	Ground (0V)
45	GPIO12	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
46	GPIO32	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
47	GPIO13	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
48	GPIO33	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
49	GND	Ground (0V)

50	GND	Ground (0V)
51	GPIO14	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
52	GPIO34	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.

53	GPIO15	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
54	GPIO35	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
55	GND	Ground (0V)
56	GND	Ground (0V)
57	GPIO16	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
58	GPIO36	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
59	GPIO17	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
60	GPIO37	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
61	GND	Ground (0V)
62	GND	Ground (0V)
63	GPIO18	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
64	GPIO38	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
65	GPIO19	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
66	GPIO39	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
67	GND	Ground (0V)
68	GND	Ground (0V)
69	GPIO20	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
70	GPIO40	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.

71	GPIO21	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
72	GPIO41	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
73	GND	Ground (0V)
74	GND	Ground (0V)
75	GPIO22	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
76	GPIO42	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
77	GPIO23	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.

78	GPIO43	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
79	GND	Ground (0V)
80	GND	Ground (0V)
81	GPIO24	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
82	GPIO44	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
83	GPIO25	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
84	GPIO45	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO18-47_VDD to 1.8V.
85	GND	Ground (0V)
86	GND	Ground (0V)
87	GPIO26	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
88	HDMI_HPD_N_1V8	Input HDMI hot plug. Internally pulled up to +1.8V via a 2.2kΩ resistor.
89	GPIO27	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-17_VDD to 1.8V.
90	ACT_LED_1V8	Internal 10kΩ pulldown to 1.8V.
91	GND	Ground (0V)
92	GND	Ground (0V)
93	DSI0_DN1	Output Display0 D1 negative

94	DSI1_DP0	Output Display1 D0 positive
95	DSI0_DP1	Output Display0 D1 positive
96	DSI1_DN0	Output Display1 D0 negative
97	GND	Ground (0V)
98	GND	Ground (0V)
99	DSI0_DN0	Output Display0 D0 negative
100	DSI1_CP	Output Display1 clock positive
101	DSI0_DP0	Output Display0 D0 positive
102	DSI1_CN	Output Display1 clock negative
103	GND	Ground (0V)
104	GND	Ground (0V)
105	DSI0_CN	Output Display0 clock negative
106	DSI1_DP3	Output Display1 D3 positive
107	DSI0_CP	Output Display0 clock positive
108	DSI1_DN3	Output Display1 D3 negative
109	GND	Ground (0V)

110	GND	Ground (0V)
111	HDMI_CLK_N	Output HDMI clock negative
112	DSI1_DP2	Output Display1 D2 positive
113	HDMI_CLK_P	Output HDMI clock positive
114	DSI1_DN2	Output Display1 D2 negative
115	GND	Ground (0V)
116	GND	Ground (0V)
117	HDMI_D0_N	Output HDMI TX0 negative
118	DSI1_DP1	Output Display1 D1 positive
119	HDMI_D0_P	Output HDMI TX0 positive
120	DSI1_DN1	Output Display1 D1 negative
121	GND	Ground (0V)
122	GND	Ground (0V)

123	HDMI_D1_N	Output HDMI TX1 negative
124	PCIE20_TXP	Output PCIE20 TX positive
125	HDMI_D1_P	Output HDMI TX1 positive
126	PCIE20_TXN	Output PCIE20 TX negative
127	GND	Ground (0V)
128	GND	Ground (0V)
129	HDMI_D2_N	Output HDMI TX2 negative
130	PCIE20_RXP	Input PCIE20 RX positive
131	HDMI_D2_P	Output HDMI TX2 positive
132	PCIE20_RXN	Input PCIE20 RX negative
133	GND	Ground (0V)
134	GND	Ground (0V)
135	USB3_HOST1_SSTXP	Output USB3_HOST1_TX positive
136	CAM0_DP0	Input Camera0 D0 positive
137	USB3_HOST1_SSTXN	Output USB3_HOST1_TX negative
138	CAM0_DN0	Input Camera0 D0 negative
139	GND	Ground (0V)
140	GND	Ground (0V)
141	USB3_HOTS1_SSRXP	Input USB3_HOST1_RX positive
142	CAM0_CP	Input Camera0 clock positive
143	USB3_HOST1_SSRXN	Input USB3_HOST1_RX negative
144	CAM0_CN	Input Camera0 clock negative
145	GND	Ground (0V)
146	GND	Ground (0V)

147	CAM1_CP	Input Camera1 clock positive
148	CAM0_DP1	Input Camera0 D1 positive
149	CAM1_CN	Input Camera1 clock negative
150	CAM0_DN1	Input Camera0 D1 negative
151	GND	Ground (0V)

152	GND	Ground (0V)
153	CAM1_DP1	Input Camera1 D1 positive
154	PCIE20_REFCLKP	Output PCIE20 ref clock positive
155	CAM1_DN1	Input Camera1 D1 negative
156	PCIE20_REFCLKN	Output PCIE20 ref clock negative
157	GND	Ground (0V)
158	GND	Ground (0V)
159	CAM1_DP0	Input Camera1 D0 positive
160	USB3_HOTS1_DP	USB HOTS1 D+
161	CAM1_DN0	Input Camera1 D0 negative
162	USB3_HOTS1_DM	USB HOTS1 D-
163	GND	Ground (0V)
164	GND	Ground (0V)
165	USB_DP	USB D+
166	PMIC_32KOUT	32.768khz output
167	USB_DM	USB D-
168	USB_OTGID	Input (3.3V signal) USB OTG Pin. Internally pulled up. When grounded the CM4S becomes a USB host, but the correct OS driver also needs to be used.
169	GND	Ground (0V)
170	GND	Ground (0V)
171	HDMI_CEC	Input HDMI CEC: internally pulled up with a 27kΩ to +3.3V.
172	PCIE20_CLKREQn_M2	Output PCIE20 CLKREQn
173	HDMI_SDA	Bidirectional HDMI SDA 5V-tolerant, requires a pullup as per HDMI specification.
174	PCIE20_WAKEn_M2	Output PCIE20 WAKEn
175	HDMI_SCL	Bidirectional HDMI SCL 5V-tolerant, requires a pullup as per HDMI specification.
176	PCIE20_PERSTn_M2	Output PCIE20 PERSTn
177	RUN(RESETn)	Bidirectional pin. Can be driven low to reset the CM4S CPU. As an output, a high signals that power is good and CPU is running. Internally pulled up to +3.3V via 10kΩ, but clamped to VBAT via a diode if VBAT is lower than +3.3V.
178	HPL_OUT	Headphone left channel output
179	PMIC_PWRON	Connect a key to GND

180	HPR_OUT	Headphone right channel output
181	GND	Ground (0V)

182	HP_SNS	Connect to GND
183	Not Connected	Can either be unconnected or +1.8V.
184	Not Connected	Can either be unconnected or +1.8V.
185	Not Connected	Can either be unconnected or +1.8V.
186	Not Connected	Can either be unconnected or +1.8V.
187	GND	Ground (0V)
188	GND	Ground (0V)
189	Not Connected	
190	Not Connected	
191	Not Connected	
192	USB_OTG_VBUSDET	VBUS voltage detection input (Connect to VBUS)
193	VDC_DET	External power adapter input detection. (for always power on)
194	VCC_BAT	Battery voltage detection input
195	SNSP (GND)	Battery current sense input+ ,When not use, connect to GND
196	SNSN (GND)	Battery current sense input- When not use, connect to GND
197	VBAT	+2.5V to +5V power input
198	VBAT	+2.5V to +5V power input
199	VBAT	+2.5V to +5V power input
200	VBAT	+2.5V to +5V power input

All ground pins should be connected.

4.1. Differential pairs

It is recommended that P/N signals within a pair are matched to better than 0.15mm. Often, matching between pairs is not so critical: e.g. HDMI pair-to-pair matching should be better than 25mm, so on a typical board no extra matching is required.

4.1.1. 100Ω differential pair signal lengths

On the CM4S all differential pairs are matched to better than 0.05mm (P/N signals).

NOTE

It is recommended that pairs are also matched on the interface board.

On the CM4S, pair-to-pairs are not always matched, as many interfaces do not require very accurate matching between pairs. Table 8 documents the CM4S track-length difference within each group. (A non-zero value represents how much longer in mm that track is, when compared to the signal with zero length difference.)

Signal	Length
CAM0_C_N	1.02
CAM0_C_P	1.07
CAM0_D0_N	0
CAM0_D0_P	0
CAM0_D1_N	2.97
CAM0_D1_P	3.00
CAM1_C_N	3.71
CAM1_C_P	3.76
CAM1_D0_N	2.57
CAM1_D0_P	2.53
CAM1_D1_N	1.97
CAM1_D1_P	1.96
DSI0_C_N	0.94
DSI0_C_P	0.98
DSI0_D0_N	0
DSI0_D0_P	0.01
DSI0_D1_N	0.27
DSI0_D1_P	0.29
DSI1_C_N	2.82
DSI1_C_P	2.82
DSI1_D0_N	0
DSI1_D0_P	0.01
DSI1_D1_N	2.09
DSI1_D1_P	2.08
DSI1_D2_N	4.15

Table 8. 100Ω differential pair signal lengths

DSI1_D2_P	4.16
DSI1_D3_N	4.08
DSI1_D3_P	4.09
HDMI_CLK_N	0.04
HDMI_CLK_P	0
HDMI_TX0_N	0.02
HDMI_TX0_P	0.04
HDMI_TX1_N	0.23
HDMI_TX1_P	0.23
HDMI_TX2_N	0.41
HDMI_TX2_P	0.36

4.1.2. 90Ω differential pair signal lengths

On the CM4S all differential pairs are matched to better than 0.05mm (P/N signals).

NOTE

It is recommended that pairs are also matched on the interface board.

Pair-to-pairs aren't always matched as many interfaces don't require very accurate matching between pairs. Table 9 documents the CM4S track-length difference within each group. (A non-zero value represents how much longer in mm that track is, when compared to the signal with zero length difference.)

Table 9. 90Ω differential pair signal lengths

Signal	Length
USB_OTG0_DP	0.03
USB_OTG0_DM	0.05
USB3_HOST1_DP	0.03
USB3_HOST1_DM	0.02
USB3_HOST1_SSTXP	0.13
USB3_HOST1_SSTXP	0.10
USB3_HOST1_SSRXP	0.07
USB3_HOST1_SSRXN	0.05

Chapter 5. Power

5.1. Power-up sequencing

The CM4S requires a VBAT (2.5V to 5V) and +3.3V supplies. Older Compute Modules required +1.8V as well; +1.8V is no longer used, but can be supplied for backward compatibility.

If the EEPROM is to be write-protected, then the EEPROM_nWP should be low before power-up.

If the CM4S is to be booted using USB, then EMMC_DISABLE_N needs to be low within 1µs of +3.3V rising.

The power-up sequence will start when +3.3V rail is above +3V. The order of events is as follows:

1. If VBAT is going to be greater than +3.3V, VBAT should rise first
2. +3.3V rises
3. VBAT rises if it is lower than +3.3V
4. RUN rises at least 10µs after the last rail to power-up.

5.2. Power-down sequencing

The operating system should be shut down before the power is removed, to ensure that the file system remains consistent. If this can't be achieved, then a filesystem like btrfs, f2fs or overlayfs (use raspi-config to enable this) should be considered.

Once the operating system has shut down, the PSU rails may be removed in the reverse order of power-up: i.e. the lowest voltage rail is removed first. Taking the RUN pin low will reset the BCM2711.

5.3. Power consumption

The exact power consumption of the CM4S will greatly depend on the tasks being run on the CM4S. Idle power consumption is typically 1.5W, but this varies considerably depending on the operating system. Operating power consumption is typically around 7W; again, this greatly depends on the operating system and the tasks being executed.

Appendix A: Troubleshooting

The CM4S has a number of stages of power-up before the CPU starts. If there is an error at any of the stages, power-up will be halted.

Bootloader

To troubleshoot the bootloader;

1. Connect a HDMI cable to see if the HDMI diagnostics screen appears.
2. Connect a USB serial cable to SODIMM pins 40 and 42 (Debug port is not connected, skip this step)
3. Short the EMMC_DISABLE_N pin to ground to force USB boot mode.
4. use **the rkdevelopment tool** download firmware to eMMC

EEPROM write-protect

The on-board EEPROM can be write-protected by shorting EEPROM_nWP to ground.

Firmware

A 5.4 or newer kernel and the latest firmware release is required. These can be updated by using usbboot to mount the EMMC as a USB MSD device.

Kernel

The updated OS images use the RK3566 Compute Module 4 SODIMM device tree file.

Appendix B: Availability

Raspberry Pi Ltd guarantees availability of the CM4S until at least **January 2031**.

Support

For documentation please see the Compute Module Hardware documentation section of the Raspberry Pi website. Support questions can be posted to the Raspberry Pi forum.

Ordering codes

Table 10. Part number options

Model	RAM LPDDR4	eMMC Storage
RK3566 CM4S	01 = 1GB	000 = 0GB (Lite)
	02 = 2GB	032 = 32GB
	04 = 4GB	064 = 64GB
	08 = 8GB	128 = 128GB
Example Part Number		
RK3566 CM4S	01	032

Table 11. Ordering options

RAM LPDDR4	Storage eMMC	SKU #	Part Number	Order Multiple	RRP
1GB	Lite	SKU0033	CM4S01000	Bulk (100 pcs)	$ 22.00
1GB	32GB	SKU0033	CM4S01032	Bulk (100 pcs)	$ 30.00
2GB	Lite	SKU0033	CM4S02000	Bulk (100 pcs)	$ 30.00
2GB	32GB	SKU0033	CM4S02032	Bulk (100 pcs)	$ 35.00
4GB	Lite	SKU0033	CM4S04000	Bulk (100 pcs)	$ 40.00
4GB	32GB	SKU0033	CM4S04032	Bulk (100 pcs)	$ 45.00

NOTE

RRP was correct at time of publication and excludes taxes.

Some options have minimum ordering qualities (MOQ), please check with your supplie